L1

Functional Checks Manual

Concise Version

PUBLICATION ISSUED BY:

Ing. C. Olivetti & C., S.p.A.
Direzione Documentazione
77, Via Jervis - 10015 Ivrea (Italy)

Title: L1 - FUNCTIONAL CHECKS MANUAL - CONCISE VERSION

Newsletter Code: 4102232 G
Date: 29-02-88
Publication Code: 4102230 T (0)
Previous Newsletters: 4102231 U

This Newsletter provides updated pages for the subject publication.

The last level completed on the attached form, Updating Status, indicates the pages to be added, removed, or replaced, the number of pages included, and the Newsletter Code. Pages marked with an asterisk should be removed from the publication. The form should be filed at the back of the publication as a permanent record of amended pages.

Each amended page is identified by the Newsletter Code shown above.
Amended pages remain valid unless otherwise noted in a subsequent Newsletter.

Summary of Amendments:

Description of the test programs aligned to the DCOS Rel.8.4.1

Ing. C. Olivetti & C., S.p.A. — Direzione Documentazione — Via Jervis 77, — 10015 IVREA (TO) Italy

Printed in Italy

Title: L1 - FUNCTIONAL CHACKS MANUAL - CONCISE VERSION

Newsletter Code: 4102233 C
Date: 30-03-88
Publication Code: 4102230 T (0)
Previous Newsletters: 4102231 U, 4102232 G

This Newsletter provides updated pages for the subject publication.

The last level completed on the attached form, Updating Status, indicates the pages to be added, removed, or replaced, the number of pages included, and the Newsletter Code. Pages marked with an asterisk should be removed from the publication. The form should be filed at the back of the publication as a permanent record of amended pages.

Each amended page is identified by the Newsletter Code shown above.
Amended pages remain valid unless otherwise noted in a subsequent Newsletter.

Summary of Amendments:

Update with 8.4.2 DCOS Release.

Ing. C. Olivetti & C., S.p.A. — Direzione Documentazione — Via Jervis 77, — 10015 IVREA (TO) Italy

Printed in Italy

L1

Functional Checks Manual

Concise Version

olivetti

PREFACE

This manual is the concise version of the L1 Functional Checks Manual (DCOS environment). It contains sufficient information to enable a technician to diagnose faults to board level and to checkout a system. The descriptions of the programs have been limited to give a general understanding of the nature of hardware faults. Also the descriptions of the interactive sections have been omitted.

Note: The A5, 4 ring binders, used to contain this document, have the following codes:

3979697 Q (2 cm)
3979698 D (3 cm)
3979699 H (4 cm)

SUMMARY

The manual, aligned to Rel. B.4.1, is divided into 19 chapters.

Chapter 1 refers to the system resident AUTODIAGNOSTICS, DIAGNOSTIC MONITOR and introduction to the FUNCTIONAL CHECKS programs. This chapter also provides the initial loading procedures that are necessary before any program can be run, these procedures are not repeated in subsequent chapters but are referred to.

Chapter 2 describes:

a) The UTLITY program which permits the operator to access various utility services in order to display the list of diagnostic programs, display, transfer and modify keyboard parameters, contents of physical sectors and copy whole or part of the diagnostic system.

b) Various programs for loading or transferring the ENVIRONMENT ACTIVATOR from one medium to another.

c) Various programs for installing the DIAGNOSTIC ENVIRONMENT from one medium to another.

Chapter 3 deals with SYSTEM RAM and SYSTEM CPU tests.

Chapter 4 deals with test programs for printer/pin-pad reader and associated controllers via various lines, encryption controllers and the M64/M70 console.

Chapter 5 deals with specific test programs for the M60.

Chapter 6 deals with video-keyboard test programs.

Chapter 7 deals with test programs for WS via MUX and ELB 3683 controllers.

Chapter 8 deals with test programs for non intelligent line controllers.

Chapter 9 deals with test programs for intelligent line controllers.

Chapter 10 deals with MFDU and FDU test programs.

Chapter 11 deals with test programs for STC and associated controllers.

Chapter 12 deals with test programs for MTU and associated controller.

Chapter 13 deals with test programs for HDU 18 MB (XU 5010) and controller.

Chapter 14 deals with test programs for HDU 14 MB (XU 5006) and controller.

Chapter 15 deals with test programs for HDU 60 MB (XU 1700) and controller.

Chapter 16 deals with test programs for HDU 120 MB (XU1703) and controller.

Chapter 17 deals with test programs for HDU via ST506 interface and controller.

Chapter 18 deals with test programs for HDU via ESDI interface and controller.

Chapter 19 deals with test programs for HDU via SMD interface and controller.

BIBLIOGRAPHY

Functional Checks Manual	- Code 4111930 B (0)
Functional Checks Manual - I/O Routines	- Code 4102070 C (0)
M34-M44-M54 - Service Manual	- Code 4105740 T (0)
M60-M60/2/3 - Service Manual	- Code 4102050 A (1)
M64-M70/2/3 - Service Manual	- Code 4111190 Q (0)

SECTORRANGE/PRODUCTS: B1/M30, M34, M40, M44, M54, M64

B2/M60, M70

DISTRIBUTION: Internal (Z)

FIRST EDITION: January 1987

CONTENTS

1. INTRODUCTION

GENERAL

The test programs described in this manual are for the Olivetti L1 system.

The basic system hardware for initiating AUTODIAGNOSTICS, loading the DIAGNOSTIC MONITOR and ANY of the FUNCTIONAL CHECKS programs comprises: CPU, RAM, video, keyboard, video-keyboard controller and a magnetic medium for loading the programs.

The magnetic medium comprises HDU, FDC, MFDC, MTU or STC and its associated controller.

The same magnetic medium must be used for loading the diagnostic monitor and the functional checks programs.

Other system configurations may be used; this is described under the heading SYSTEM CONFIGURATION of this section and, if there are any specific hardware requirements, in the description of the individual functional checks programs.

OVERVIEW

The **autodiagnostic** is resident on cpu rom and is used to check the system ram, system configuration, the initial program loading device and initiate the loading of the customer operating system (OS) or the diagnostic monitor.

The tests are started automatically on power-up and any errors are indicated by a code either on the console or on the video. Fault detection is limited to board level.

The customer operating systems available are in the following environments: emulated and native (provisions are made for the addition of other environments). These systems are not covered in this manual.

The **diagnostic monitor** is a particular type of operating system which provides an interactive diagnostic system and the means for loading the functional checks programs.

The functional checks programs provide the individual tests for checking the operation of a particular system or peripheral and provide trouble shooting facilities.

The diagnostic monitor is loaded from a magnetic medium (as defined above) into system ram using a bootstrapper which is also located on the same magnetic medium.

The bootstrapper is loaded into system ram either by the system rom or by the environment activator as is the case with some HDUs.

The environment module is located on the same magnetic medium as the diagnostic monitor, it is loaded into system ram where it is used to designate and enable the workstation to be used, locate and load the bootstrapper of the required operating system.

SYSTEM CONFIGURATION

The overall system configuration for connecting the available facilities is shown in figure 1-1. The facilities indicated are not the complete range of the OLIVETTI L1 system as only the boards which are commonly used have been documented.

The following points must be observed:

1. The parameters for ETS workstation, VT100 video and M24 PC interface are as follows:
   - Baud rate = 9,600
   - Bits/char = 7
   - Stop bits = 1
   - Parity = even
2. Standard workstations must be connected to channel 1 of the first Multiplexer in the configuration and work with the following default parameters:
   - Baud rate = 9,600
   - Bits/char = 8
   - Stop bits = 1
   - Parity = odd
3. The VT100 and PC M24 must be connected to channel 0 and each have its line parameters set (see description of monitor help procedures, item 9) MUX parameters).

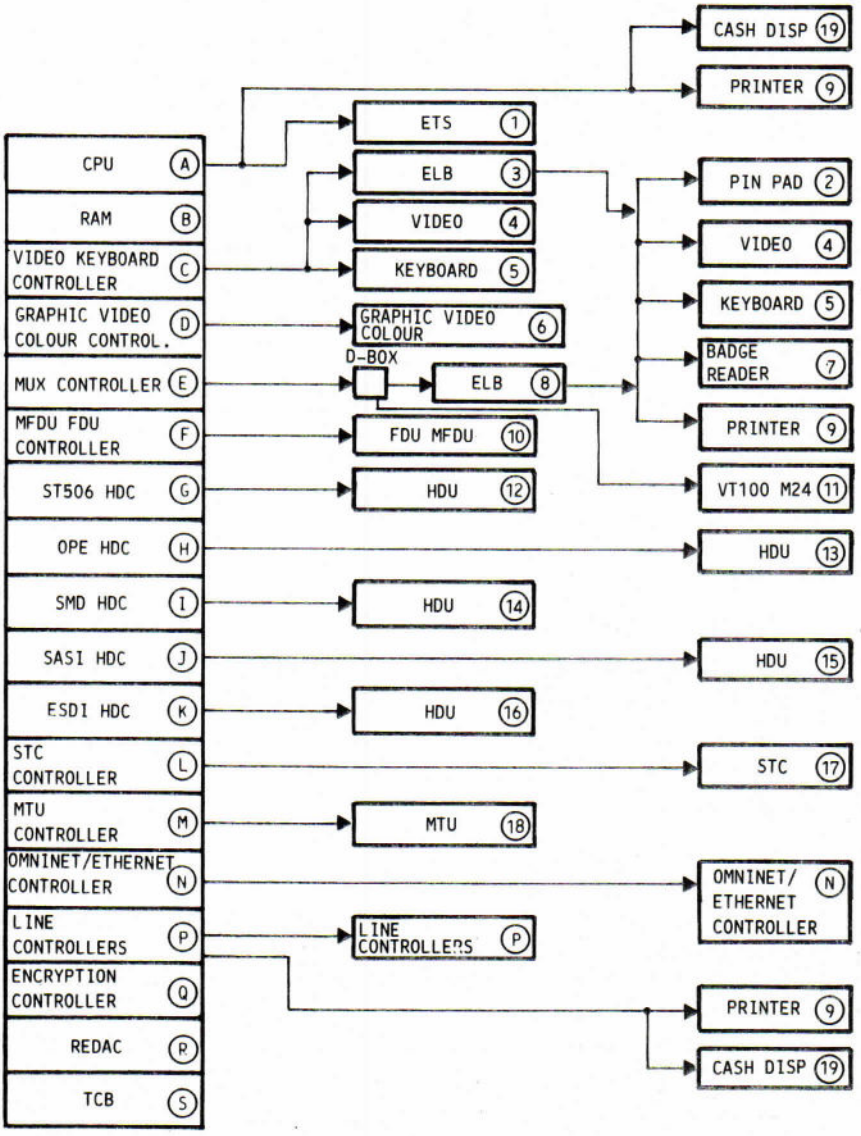


Fig. 1-1 SYSTEM CONFIGURATION

N.B.

Two or three CPU's can be used for M60/2 and M60/3 systems.

SYSTEM CONFIGURATION TABLE

ITEM	COMPONENT
A	CPU : UC036 M30/M40 UC042 or UC042/A M30/M31/M40 UC048 M34/M44 UC070 M54/M64 UC040 M60 UC071 M70
B	RAM : ME019, ME024, ME027, ME032, RA57/A-B-C-E, RA057, RA800, RA800/A, RA80/A-B-C-D-F-N, RA65, RA65/B CACHE: UC041
C	VIDEO/KEYBOARD CONTROLLER:G0157, G0252, G0224 (A/N) G0207 + G0157 (Graphic) G0255 + G0252 (Graphic)
D	GRAPHIC VIDEO COLOUR CONTROLLER: G259 + G0260 + G0261
E	MUX CONTROLLER: G0322
F	MFDU/ FDU CONTROLLER: FOR XU4301: G0184 + G0182, G0217 + G0182, G0229, G0240, G0280/A-C-E FOR XU4350: G0280/E FOR XU4305: G0229, G0280, G0280/B-D, FOR NDOB DE: G0280/D FOR XU6030: G0184 + G0182, G0217 + G0182, G0229, G0280, G0280/B-D
G	HDU CONTROLLER, ST506 INTERFACE: G0363
H	HDU CONTROLLER, OPE INTERFACE: G0230 + G0231/A
I	HDU CONTROLLER, SMD INTERFACE: G0301/A + G0302/A
J	BUS ADAPTER, SASI INTERFACE: G0298 + G0299

ITEM	COMPONENT
K	HDU CONTROLLER, ESDI INTERFACE: G0404 + G0405
L	STC CONTROLLER: FOR XU1120: G0200/B + G0201/B FOR XU1130: G0200/B + G0342 FOR ARCHIVE 5945C (45/60 MB): G0417 + G0418
M	MTU CONTROLLER: G0278/B
N	ETHERNET CONTROLLER: G0212/A; OMNINET CONTROLLER: G0308
P	LINE CONTROLLERS: TWIN RS232/CL UNIT: G0151, G0327 (FAST) V24 LCU: G0156: G0300 (FAST) LION 9.6 LCU: G0234, G0333 (FAST) LION200/V24 LPU: G0256 (DED. SEG), G0340 (SHARED) V24/V24 DUAL LPU: G0236 (DED. SEG), G0331 (SHARED) TW422 LCU: G0264, X24 LCU: G0303 LION 9.6/V24 LPU: G0340/A MOIN 5.1: IF092 MOIN 5.2: IF192
Q	ENCRYPTION CONTROLLER:G0257, G0257/B FOR PIN-CHECK G0257/C (CAT ALGORITHM)
R	REDAC MR: C0099
S	TIMING CONTROLLER BOARD: TCB82 FOR M60

ITEM	COMPONENT
1	ETS WS: ETS 1010/2010
2	PIN-PAD CONTROLLER: G0195; PIN-PAD UNIT: PIN1440
3	ELB 1381: IF099/IF141, ELB 1382: G0189/G0269
4	VIDEO B/W A/N: DSM1205 5"; DSM1219 15" TRIV.; DSM1209 9" DSM1215 15"; DSM1219 9" TRIV. VIDEO GRAPHIC: DSM1216 15" VIDEO COLOUR A/N: DSM1214 14"
5	KEYBOARD: ANK14XX, NKB14XX, AKB14XX
6	VIDEO GRAPHIC COLOUR: DSM1244
7	BADGE READER MBR1932/MRW1810
8	ELB 3683: BA126/G0239
9	PRINTER: ANY OLIVETTI L1 PRINTER
10	MFDU: XU4301 320KB, XU4350 320KB SLIM, XU4305 1MB ND08 DE 1MB SLIM FDC: XG 6030
11	VT100/ PC M24
12	HDU: XM5221/2 20 MB, XU1707 27 MB, XU 1709 65MB MICROPOLIS 1323, 1323/A 40MB, XU5006 14 MB
13	HDU: XU5010 18 MB

14	HDU: XU1700 60 MB; XU1703 120MB; PATRIOT 275 MB (SMD INT.)
15	HDU: XU5006 14 MB WITH DTC510 BP/BO CONTROLLER (ST506 INT.)
16	HDU: CDC WREN3 140 MB; MICROPOLIS 1355 140MB; FUJITSU M2246 140 MB (ESDI INT.)
17	STC: XU1120 20 MB; XU1130 20 MB CYPHER or ARCHIVE 9020B; XU4950 45/60 MB ARCHIVE 5945C
18	MTU: XU1705 40 MB
19	CASH DISPENSER: CA2000

1.1 AUTODIAGNOSTICS

1.1.1 STRUCTURE

The autodiagnostics comprises the following activities:

- CPU TEST
- SYSTEM RAM TEST
- SYSTEM CONFIGURATION TEST
- IPL SCHEDULING
- IPL DEVICE AUTODIAGNOSTICS
- ENVIRONMENT ACTIVATOR LOADING
- BOOTSTRAP LOADING

1.1.1.1 CPU TEST

The purpose of this test is to check the integrity of the CPU components involved in Initial Program Loading (IPL).
It is divided into the following tests:

- Z8001 (CU) TEST
- ROM TEST
- Z8010 (M.M.U.) test

Z8001 (CU) TEST

By successfully executing the rom-loader, the following are tested: the system clock, the + 5V supply, the CPU data/address busses, NMI signals, seg-traps, bus request etc., and the code "1" is sent the console. If the rom-loader is interrupted this is indicated by no diagnostic code being sent to the console.

ROM TEST

The test checks the CRC in the ROMs, using the MAMO-ROMK cyclic calculation algorithm.
If an error occurs, the program is interrupted and the code "1" remains displayed on the console.

Z8010 (M.M.U.) TEST

All the segment descriptor registers are read and written to in this test. If an error occurs, the program is interrupted and the code "1" remains displayed on the console.

If the test is successful the segments which address the ROM, the ROM-board (where the resident debugger is located) and the RAM of the video controllers are programmed.

The following tests are run on these controllers before they can be used:

a) RAM test resident on the controller

b) Display Synchronisation test.

If these tests fail on any of the display controllers, the "diagnostic state" variable relative to that controller is initialised at value %ffff in the "device-table" (see section on SYSTEM CONFIGURATION TEST).

1.1.1.2 SYSTEM RAM TEST

The test determines the PHYSICAL LOCATION and capacity of the SYSTEM RAM and then performs a SHIFTING PATTERN test on the RAM.

RAM PHYSICAL LOCATION TEST

The "READY" signal is used to access the first address of the SYSTEM RAM. The capacity of the RAM is then determined as the RAM is arranged without any addressing discontinuity even when several RAM boards are used in a system.

At the start of the RAM test the code "2" is displayed on the console and video. If the "READY" signal is not present during an access, or an address area of less than 16 Kbytes is found (RAM board NOT present or faulty), a non maskable interrupt is generated and the code "2" remains displayed on the console and video.

If the test completes successfully, the MMU (Z8010) is programmed.

SHIFTING PATTERN TEST

After programming the MMU the RAM is tested with a shifting patterns.

If errors are found the section of RAM containing the largest block of good contiguous memory space is used as the SYSTEM RAM and the MMU is reprogrammed accordingly. If this block is less than 16 Kbytes, the program is interrupted and the code "2" is left displayed on the console and video.

If the RAM test completes successfully, the following parameters are initialised:

start RAM physical address
end physical address
start good RAM physical address
end good physical address

Each of these parameters comprises a word containing the most significant and intermediate address byte.

1.1.1.3 SYSTEM CONFIGURATION TEST

The SYSTEM CONFIGURATION is determined by a procedure which selects the "type" port of each slot and which compiles the "devices-table". The "devices-table" contains information on the type of boards inserted in the various slots of the system and the response to the autodiagnostics of the various controllers.

If the controller inserted in a slot responds when the type port of the slot is accessed, the parameters of the "devices-table" reserved for that slot are set to "0"; otherwise the whole field reserved for the slot is set to %FFFFFFFF.

NOTE:

If a controller does NOT give the ready signal then the controller is indicated NOT present or missing (%FFFFFFFF) in the device table.

The system configuration is displayed after the AUTODIAGNOSTICS have been successfully completed and the MONITOR correctly loaded. An example of the system configuration table is given in the description of the MONITOR HELP procedures section 1.2.3.3 function No 8.

1.1.1.4 IPL SCHEDULING

An IPL scheduler is used to select the device with the highest priority of all the IPL devices in the system and to activate program loading from that device. This is done by first searching for the device from the lowest I/O addresses (slot #0 onwards) and from unit "0" onwards and then, using the ROM loader, loading the first program.

Operations continue depending on the device type (primary or secondary) and on the program used to load the ENVIRONMENT ACTIVATOR on HDU:

a) For the FDU's, MFDU's, STC's and MTU's (secondary devices) the first program loaded is the BOOTSTRAPPER. If loading is successful the ROM loader relinquishes control to the BOOTSTRAPPER. The BOOTSTRAPPER then in turn, subject to the results of the autodiagnostics, loads the MONITOR (in this case the DCOS environment) or the OS.

   If the BOOTSTRAPPER is NOT loaded successfully, the scheduler selects the next device (in order of priority) and repeats the above operation, recycling if necessary.

   The number of attemps at loading the BOOTSTRAPPER is limited to eight in order to avoid damaging the device.

b) For HDU's (primary devices) the first program loaded is the ENVIRONMENT ACTIVATOR. This module is used to load the BOOTSTRAPPER as described in the section headed ENVIRONMENT ACTIVATOR LOADING.

   Once the BOOTSTRAPPER has been loaded into SYSTEM RAM, the ACTIVATOR module relinquishes control to the BOOTSTRAPPER to load the MONITOR or the OS.

IPL PRIORITY

The following is a list of IPL peripherals in order of priority:

primary-devices	HDU with SMD interface
	HDU 18MB OPE
	HDU with ST506 interface
	HDU with SASI interface
secondary-devices	FDU
	MFDU
	STC
	MTU

DEVICE SELECTION

The selection of the type of device is determined by the position of the IPL switch on the console.

With the switch in the "primary" position, the whole table of IPL devices is scanned.

With the switch in the "secondary" position, only the table of IPL devices from secondary devices is scanned.

1.1.1.5 IPL DEVICE AUTODIAGNOSTICS

The IPL device autodiagnostics are in two parts; the initialization phase, and the read phase.

During initialization, the controller status is checked following specific commands and interrupts.

An error in the initialization phase causes a faulty controller message (blinking error code "1").

During the read phase, the magnetic medium is read and the data transfered into SYSTEM MEMORY. If there are any errors during this phase due to the peripheral a blinking code "2" is displayed on the console or if the error is due to the medium (e.g. tape/diskette) then a blinking error code "4" is displayed on the console.

At the end of the read command a further test is made to check that the DMA transfer has been correctly executed, as follows:

a) A maximum of 120 locations of the read buffer is checked to see if it still corresponds with the test pattern written before the read command.

b) If this is not so, the controller error code blinking "1" is issued.

1.1.1.6 ENVIRONMENT ACTIVATOR LOADING

GENERAL

The ENVIRONMENT ACTIVATOR is a software module resident on the HDU, as follows:

a) On sectors 0 to 6 where the ENVIRONMENT ACTIVATOR has been loaded using the LDHS2 program,

b) On sectors 0 to 6 and a sector of 64 kbytes located in the user area indicated by Pointer Label SWBOOT (found in sector 9), where the ENVIRONMENT ACTIVATOR has been loaded by the LDHMU2 program.

If the resident AUTODIAGNOSTICS is succesful, the ENVIRONMENT ACTIVATOR is loaded into the SYSTEM RAM using ROM and transfers started.

The module loads the BOOTSTRAP of the environment OS, selected through a key code or by default.

The environment OS available are: EMULATED, NATIVE, DIAGNOSTIC MONITOR and OTHERS (reserved area for additional environments).

OPERATION OF THE ENVIRONMENT ACTIVATOR MODULE

The Environment Activator resident in system RAM segment 32 performs the following activities:

1. Programs a Scratch segment of at least 4 Kbytes in which the Operating System bootstrap code number is placed

2. Identifies the type of controller on which the IPL is taking place

3. Designates and enables the Workstation to be used. The search algorithm chooses the first STANDARD WS in M30/34 and M40/44 systems or the last one in an M60. If the STANDARD WS is not found, the algorithm selects in the following order:

   - KDC (video-keyboard controller),
   - graphic colour video,
   - ETS workstation,
   - the WS connected to channel 1 (current loop) of the first multiplexer found,
   - the VT100 or M24 connected to channel 0 (RS232) of the first multiplexer found,

4. Examines the 3 HDU sectors 7, 8 and 9, the contents of which are the volume, OS environment label and pointer label.

5. If system is UNATTENDED:

   loads the bootstrap of the OS currently active on the system. If no OS is active at that time, error code "E" will be displayed both on the video and the diagnostic console.

6. If system is ATTENDED:

   enables the keyboard automatically (when the bootstrap is of the first OS active) and displays the following menu on the video:

```
            SELECTOR......R. :X.Y.)

            x yyyy  z......= 10
            x yyyy  z......= 11
            x yyyy  z......= 15

            SELECT O.S. (OR DEFAULT)
```

   where:

   - (R. X.Y) = the release update level

   -

x = the environment code name

- yyyy = the commercial name of the OS installed
- z = 1 if the environment is active; = 0 if it is not active
- 10, 11...15 = code numbers given to the various HD environments. The operating systems are presented in their label order.
- (Default) indicates the first OS active, which is issued if no other environmental code is entered.

NOTE:

The DCOS environment is not included in the menu.

The operator has approximately 5 seconds from the time SELECT the OS (OR DEFAULT) is displayed to select the operating environment.

If no code is entered, the first OS active on HD is bootstrapped.

If there is no active OS, error code "E" is displayed on both the video and diagnostic console.

For the diagnostic environment, the code number to be entered is "50".

After a code has been entered, the following cases may arise:

- if assigned key code is already loaded, the OS selected is still loaded
- if an unscheduled code is entered, the program is interrupted and the error code "E" is displayed both on video and the diagnostic console.

1.1.1.7 BOOTSTRAP LOADING

The bootstrapper is the module which once loaded successfully into the SYSTEM RAM takes over control from the ROM LOADER (for secondary devices) or from the ENVIRONMENT ACTIVATOR (for primary devices).

The floppy disk driver uses the information from the ERMAP and volume label for further reads (RAM bootstrapper). For this, the system disk must conform to System Standard no. 17.

Finally, to implement the subsequent loading steps activated by the bootstrapper, the ROM offers the following routines:

a) multitrack read routine

b) read track "0" floppy disk routine

c) diagnostic output

1.1.2 DIAGNOSTIC MESSAGES

All ROM software activity is identified by a diagnostic code displayed on the system console. There are two types of console, and the codes sent to each type are shown below.

1.1.2.1 M30/M34/M40/M44 CONSOLE

This console has a single digit display. The diagnostic message is shown in two phases: during the initial steps of the AUTODIAGNOSTICS, just before IPL, by a single non blinking character, after IPL by four blinking characters. The characters are interpreted as follows:

First Phase: Non Blinking Code

Code	Description of error
1	CPU board fault
2	system RAM fault
3	interrupt time vector not expected
4	ROM-DEBUGGER activated (if present)
5	wait for outcome of first IPL attempt
6	segment trap after activating bootstrapper
7	non maskable interrupt after activating bootstrapper
8	unimplemented instruction after activating bootstrapper
A	privileged instruction after activating bootstrapper
B	system call after activating bootstrapper
C	non vectored interrupt after activating bootstrapper
D	wait for IPL switch (approx. 3 secs.) in order to activate the "Total Memory Dump" procedure. If the IPL is not switched, or if the "Total Memory Dump" handling module (resident in RAM) cannot be accessed, the test continues with the normal IPL.

Second Phase: Blinking Code

These error codes relate to exchanges with the IPL controllers.
The characters shown below are emitted at intervals of approximately one second:

" . X Y Z "

and have the following meaning:

"." [full stop] error code interpretation synchronization symbol

"X" error code with the following meaning:

"X" = 1 controller board fault

= 2 peripheral fault (e.g. disk drive unit)

= 4 medium read fault (e.g. diskette/tape damaged or NOT formatted correctly)

= 8 medium [disk/tape] not inserted or medium without operating system (e.g. SYSO or DIAG missing at the start of the magnetic medium - see section 1.1.1.7)

"Y" relevant controller slot name

"Z" faulty unit

1.1.2.2 M60 CONSOLE

As the M60 system console has a four digit display, both phases of the diagnostic message are shown by non blinking error codes, interpreted as follows:

First Phase

Code	Description of error
. 1	CPU board fault
. 2	system RAM fault
. 3	interrupt time vector not expected
. 4	ROM-DEBUGGER activated (if present)

Code	Description of error
. 5	wait for outcome of first IPL attempt
. 6	segment trap after activating bootstrapper
. 7	non maskable interrupt after activating bootstrapper
. 8	unimplemented instruction after activating bootstrapper
. A	privileged instruction after activating bootstrapper
. B	system call after activating bootstrapper
. C	non vectored interrupt after activating bootstrapper
. D	wait for IPL switch (approx. 3 secs.) in order to activate the "Total Memory Dump" procedure. If the IPL is not switched, or if the "Total Memory Dump" handling module (resident in RAM) cannot be accessed, the test continues with the normal IPL.

Second Phase

The code is expressed by the following characters:

" . X Y Z "

which are interpreted as follows:

"." [full stop] error code interpretation synchronization symbol

"X" error code with the following meaning:

"X" = 1 controller fault

= 2 peripheral fault

= 4 medium read fault

= 8 medium [disk/tape] not inserted or medium without operating system

"Y" relevant controller slot name

"Z" faulty unit

1.1.2.3 OUTPUT ON THE VIDEO DISPLAY

The codes shown on the system console are also shown on the system display, as follows:

1) code expressed by a single digit

```
C    rel. X.Y
```

where: C = number indicating the error code
X.Y = " " the rom-loader release

2) code expressed by three digits

```
A B C    rel. X.Y
```

where: A B C = number indicating the error code
X.Y = " " the rom-loader release

1.1.3 ROM INTERFACE MULTIPROCESSOR

M60 multiprocessor systems (where more than one CPU are used) are handled by the CPU ROM as follows:

1. The ROM checks whether the CPU is MASTER (i.e. connected to REDAC) by examining the DIP switches on the CPU board (all four switches should be closed). If it is MASTER, the CPU and RAM autodiagnostics are run, and then the IPL is performed (as normally occurs with a single processor).

2. On SLAVE CPUs which are not connected to REDAC, only the CPU autodiagnostics are run and then the RAM size is determined so that segment can be mapped on the last K-byte of RAM for all the MMUs on the SLAVE boards.

3. The MASTER CPU which executed the system IPL should at the end of the DIAGNOSTICS:

   a) Load into memory the code for the other CPUs to execute

   b) Initialize the Inter Processor Communication (IPC) parameters in RAM

   c) Send the IPC command to the other CPUs.

NOTE: the IPC parameter area is common to all the CPUs present in the system.

1.2 DIAGNOSTIC MONITOR

FOREWORD

The DIAGNOSTIC MONITOR is a program which contains the DIAGNOSTIC ENVIRONMENT OPERATING SYSTEM. This program must be installed in the SYSTEM RAM before any of the FUNCTIONAL CHECKS programs can be accessed.

Before the program can be loaded into SYSTEM RAM the AUTODIAGNOSTICS described in section 1.1 must be successfully completed.

The SYSTEM CONFIGURATION for loading the MONITOR is as described in section 1.

PROGRAM PURPOSE

To provide an OPERATING SYSTEM (OS) to test a machine and its peripheral and to provide the following facilities:

- the means of loading the FUNCTIONAL CHECKS program chosen by the operator from the diagnostic library.
- the means of modifying the operation of the program and individual tests by use of MONITOR HELP commands in order to test the system interactively, recycle/omit tests and modify operating parameters.
- the means of selecting tests by using the individual PROGRAM MENUs.
- the means of displaying the FUNCTIONAL CHECKS program library.

1.2.1 DIAGNOSTIC MONITOR LOADING PROCEDURES

The DIAGNOSTIC MONITOR is loaded automatically on switch-on after the AUTODIAGNOSTICS have been successfully completed. When the DIAGNOSTIC MONITOR has been correctly loaded the SYSTEM CONFIGURATION is displayed on the video.

1.2.2 MONITOR ACCESS PROCEDURES

Once the DIAGNOSTIC MONITOR has been loaded into SYSTEM RAM it can be accessed by hitting ENTER after which the system goes into MONITOR ENVIRONMENT and the MONITOR MASK is displayed.

The MONITOR MASK is essentially a MENU which lists the functions available in MONITOR ENVIRONMENT. These functions permit the FUNCTIONAL CHECKS programs to be loaded (or re-loaded) into SYSTEM RAM, the program library to be displayed and the MONITOR HELP to be accessed.

MONITOR ENVIRONMENT

The MONITOR ENVIRONMENT procedures are indicated in figure 1-2 and may be carried out as follows:

FUNCTIONAL CHECKS PROGRAM LOADING (LOAD on MENU)

1. Type 1XYZ + ENTER where XYZ = program code (If code less than 100, X =0; If code less than 10, XY =00).

OR

1. Type 1 + ENTER to load the LOAD module.

   When the LOAD module has been loaded, the program code request is displayed on the video.

2. Type the program code + ENTER to load the program.

In both cases refer to section 1.2.4 for PROGRAM EXECUTION in DIAGNOSTIC ENVIRONMENT.

PROGRAM LIBRARY ACCESS (MAP on MENU)

1. Type 2 + ENTER to select MAP (PGMS)

2. Hit ENTER to return to MONITOR (if on last page) or turn page (if NOT on last page).

MONITOR HELP ACCESS (HELP on MENU)

Type 3 + ENTER to go into HELP, then refer to section 1.2.3. for MONITOR HELP ENVIRONMENT.

PROGRAM RE-RUN (if already loaded; GO on MENU)

Type 4 + ENTER, then refer to section 1.2.4.

RESPONSE TO ERRORS IN MONITOR ENVIRONMENT

The system responds to an incorrect procedure as follows:

a) If a number other than 1, 2, 3 or 4 is entered, the MONITOR MASK is displayed again.

b) If the GO program is selected (4 + ENTER hit) before the LOAD program has been loaded (1 + ENTER hit or 1XYZ + ENTER hit), the Monitor mask is displayed again.

c) If the disk containing the test program is removed before the program required is loaded, the following message is displayed:

   *** HALT DML UNIT ***

To continue, hit "ENTER", re-insert disk and repeat program loading procedures.

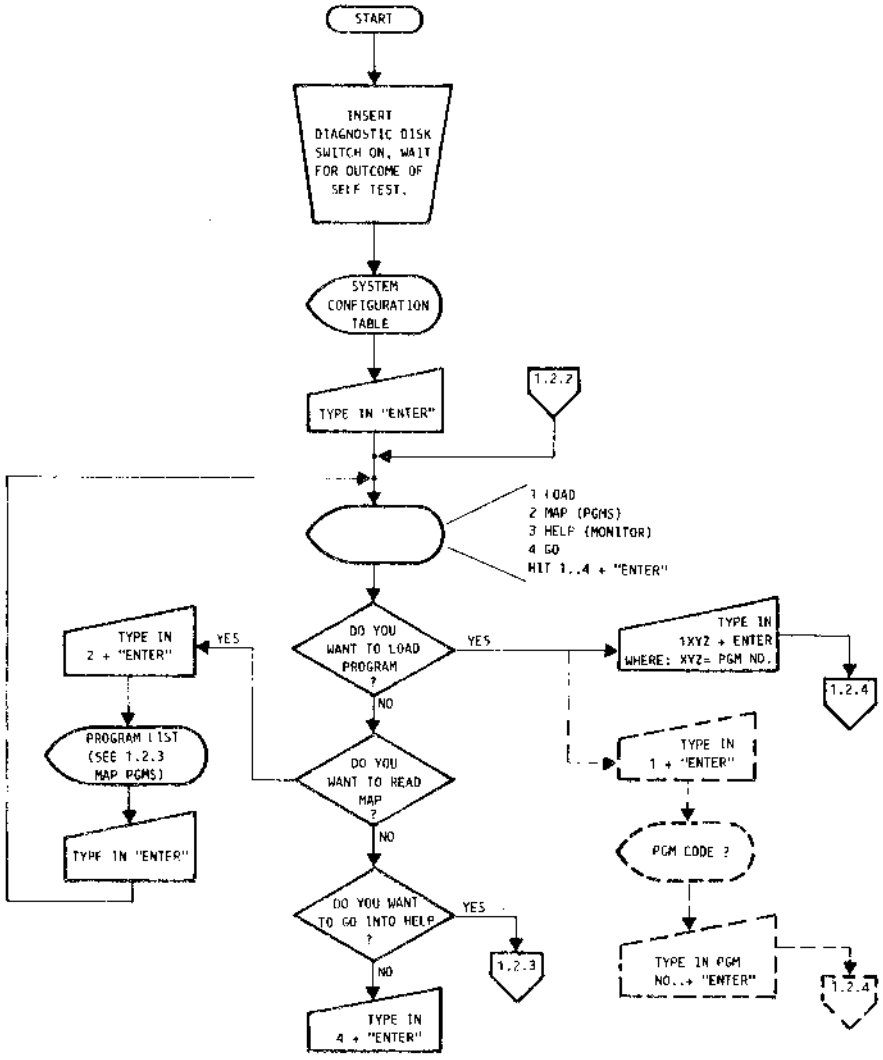


Fig. 1-2 DIAGNOSTIC MONITOR Loading - MONITOR ENVIRONMENT Procedures

1.2.3 MONITOR HELP ENVIRONMENT

1.2.3.1 Foreword

MONITOR HELP ENVIRONMENT is a special MONITOR state which provides the operator with a list of MONITOR commands and the information needed to carry them out. It is accessed in MONITOR ENVIRONMENT (when MONITOR MASK is displayed) by hitting 3 + ENTER. The commands are used for the following functions:

1. To access the list of programs in the library.
2. To load a program from the library.
3. To run a previously loaded program.
4. To set the activation modes for:
   - preprogram
   - program loop
   - test loop
   - diagnostic program chains
   - cache status
   - level of messages to operator
5. To set the following operating modes:
   - stop error
   - trace
   - debugging
   - diagnostic level
6. To establish the medium for the status/error messages:
   - hard copy
   - video
7. To display the hardware configuration of the machine under test.
8. To modify the set-up parameters of the multiplexer.

1.2.3.2 Operating procedures

The HELP MENU is shown in Fig.1-3. A function from the menu is selected by hitting the number shown adjacent the function required, plus "ENTER". Hit ENTER only to select the next page of the MENU or if on last page to return to MONITOR.

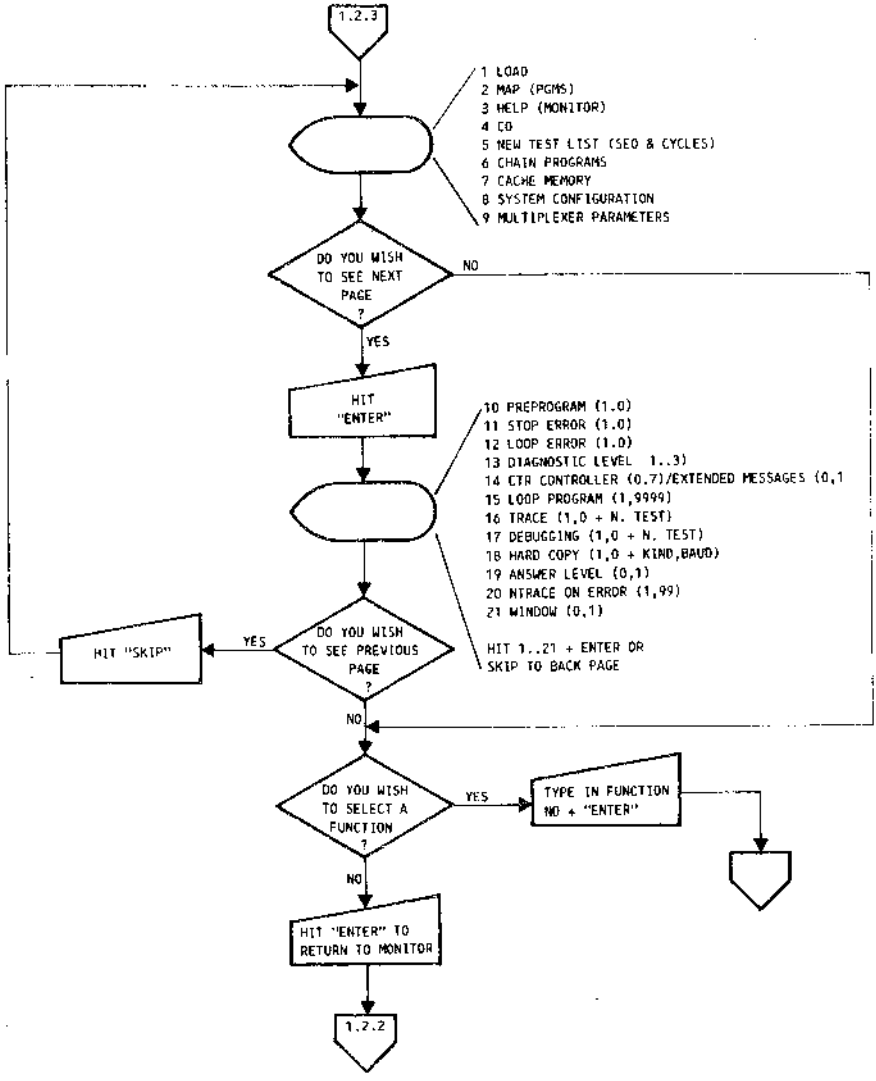


Fig. 1-3 Monitor Help Procedures

1.2.3.3 Description of the MONITOR HELP procedures

Foreword

The procedures described below are given the same numbers as in the menu seen in figure 1-3.

1 LOAD

This command permits the program to be loaded into SYSTEM RAM. Once initiated a request to enter the program code is displayed on the video. The program code should then be typed out and ENTER hit. However, unlike the LOAD command in MONITOR ENVIRONMENT, loading is NOT followed by program activation; instead, control is returned to the HELP for activation of further commands.

2 MAP (PGMS)

This command gives a list of the programs available, specifying for each, in the order shown:

- CODE (3 chars.): Program code number
- FILENAME (6 chars.): Program name
- REL (2 chars.): Release
- TR/ST (4 chars.): Starting Track and Sector (for floppy,minifloppy)
  Logic sector; this is the offset value from the beginning of the reserved diagnostic area (for HDU)
  Logic block, the offset value (for STC or MTU).
- LENGTH (3 chars.): Program length in sectors (of 256 bytes)
- DATE (6 chars.): Date catalogued (Day-Month-Year)

Hit ENTER for next page/DIAGNOSTIC MONITOR

3 HELP (MONITOR)

The command has no effect if activated (as system is already in MONITOR HELP).

4 GO

This is the command to run a program previously loaded in RAM via the LOAD command.

5 NEW TESTS LIST (SEQ.& CYCLES)

This command cannot be activated with Release 8.0 programs, but may be used with programs prior to Release 6.0. It permits the test sequence and the cycle number to be altered.

The default sequence AAXXBBYYCCZZ is displayed, where:

AA,BB,CC,...= code numbers identifying the individual tests of the test program (2 figures)
XX,YY,ZZ,...= number of loop cycles requested per test, AA, BB, CC etc., respectively.

Type in NEW TEST LIST + ENTER to continue.

WARNING

The NEW TEST LIST is NOT activated until the program is loaded via the LOAD command

6 CHAIN PROGRAMS

This command is used to string together a number of diagnostic programs which will be run with the default parameters and without any operator intervention. The resulting chain can be either temporary or permanent, i.e. recorded on magnetic medium. When this command is activated, the following message will be displayed on the video:

```
give me your programs sequence using the codes + ENTER for each one
use "SKIP" to get off
```

Type in CODE NO + ENTER for each program to be chained then ENTER only to close input or hit SKIP if chaining is NOT required.

When the chain has been entered, the monitor displays a new request:

```
Do you want to write chain on FDU ?
(0 = no 1 = yes "SKIP" = no-chain")
```

- If 0 is entered, the chain is not recorded on floppy disk and therefore is NOT permanently recorded i.e. remains recorded until system reset or until the operator re-selects the CHAIN command and hits SKIP for no-chain selection.
- If 1 is ENTERED, the chain entered is recorded on floppy disk and is only removed when the operator goes into HELP, selects CHAIN command and hits SKIP for no-chain selection.
- If SKIP key is hit, chain entered is ignored.

ERROR SIGNALS

When the IPL is made from STC or MTU, an attempt to record the chain will receive the following response:

```
sorry, I cannot write on STC/MTU unit
```

7) CACHE MEMORY

This function is used only on M60, M64 and M70. It is used to find out or modify the CACHE MEMORY status. When the function is activated, the following message is displayed:

```
CACHE MEMORY IS   ENABLED/ DISABLED

HIT ENTER TO CONTINUE
```

Hit ENTER only to accept the status indicated or hit 1 + ENTER to ENABLE the CACHE memory or 0 + ENTER to DISABLE the CACHE memory.

N.B. The MONITOR when loaded initially disables the CACHE memory.

8) SYSTEM CONFIGURATION

This function displays the system configuration table. An example is shown below:

```
-------------------------------------------------------------------------
  (xx.yyy.zzzz)     SYSTEM ENVIRONMENT      RAM SIZE   wwww KB

 0 XX-YYYY           1 XX-YYYY           2 XX-YYYY           3 XX-YYYY
 4 *******           5 *******           6 *******           7 *******
 8 *******           9 *******          10 *******          11 *******
12 *******          13 *******          14 *******          15 *******
16 *******          17 *******          18 *******          19 *******
-------------------------------------------------------------------------
```

HIT ENTER TO CONTINUE

where:

- The 1st line gives the release date (xx.yyy.zzz) and memory size (wwww) in KB.
- The next 5 lines (4 in M 40) give board details where:

. XX = type of controller inserted in slot indicated

. YYYY = results of the autodiagnostic tests

The configuration table is drawn up during the loading controller search phase (see SYSTEM CONFIGURATION TEST section 1.1.1.3) when the slots in the board housing are scanned.

In this phase the video controllers are programmed for use as diagnostic output devices.

Controller programming is conditioned by a video control logic test. If the results are satisfactory, the controller diagnostic response word is set to "%0000"; otherwise, it is "%FFFF".

The CPU board is always in 16th position.

The table below lists various types of controllers:

CONTROLLER	LOGIC NAME
CENTRAL UNIT	FF
TIMING CONTROL BOARD	F8
ENCRIPTION AND RTC CONTROL BOARDS	21
REAL TIME CLOCK CONTROL BOARD	20
VIDEO-KEYBOARD CONTROLLER (ALL)	FE
GRAPHIC VIDEO EXPANSION	FD
PIN PAD/BADGE READER CONTROLLER	B0
TWIN RS 232/C.L. CONTROLLER	CF
TWIN RS 422 CONTROLLER	DB
ENCRIPTION CONTROLLER	33
"V24" LINE CONTROLLE	D2 UNATTENDED D3 NORMAL
"X21" LINE CONTROLLER	D5
LION 9.6 LINE CONTROLLER	D7
"V24 + V24" LINE CONTROLLER	22 FULL SEGMENT 28 HALF SEGMENT
"V24 + LION200" LINE CONTROLLER	23 FULL SEGMENT 27 HALF SEGMENT
LION 9.6 LINE CONTROLLER	25 FULL SEGMENT 26 HALF SEGMENT
ETHERNET LINE CONTROLLER	6F FULL SEGMENT 7B HALF SEGMENT
OMNINET LINE CONTROLLER	6B
MULTIPLEXER CONTROLLER	30
GIPO IEEE 488 CONTROLLER	EF
HDU INTEGRATED CONTROLLER (OPE)	E4
STC (20 MB) CONTROLLER	E6
STC (45/60 MB) CONTROLLER	E7
FDU/MFDU CONTROLLER (1 MB)	E1
MFDU CONTROLLER (320 KB)	E0
"TTL" LINE CONTROLLER	D0 UNATTENDED D1 NORMAL
FUJITSU HDU CONTROLLER (SMD)	61
HDU CONTROLLER (ST506)	65
HDU CONTROLLER (ESDI)	66
CIPHER MTU CONTROLLER	62

9) MULTIPLEXER PARAMETERS

This command permits the operating parameters of the MUX lines to be modified, so that a VT100 or a PC M24 can be connected and used as work stations or a STANDARD WS connected.

The only keys used, other than the number keys on the VT100 or PC M24, are the following:

- CR KEY to ENTER
- ESCAPE KEY to SKIP
- BACK SPACE to CANCEL

When command 9 is selected the set-up default parameters are displayed as follows:

```
CHOOSE REQUIRED PARAMETERS

                          WS    OTHERS

    LINE NUMBER            1       0
    MODE                   2       1
    PARITY               odd    even
    STOP                   1       1
    LENGTH                 8       7
    SPEED               9200    9600

HIT 1 (WS) OR 0 (OTHERS) + ENTER
HIT ENTER TO WRITE PARAMETERS
```

Hit 1 then ENTER if operating on STANDARD WS or 0 then ENTER if operating on other WS (VT100 or PC M24).

In order to work on a VT100 or PC M24, as well as modifying the minitor set-up parameters, the terminal must also be aligned to DCOS environment. The VT100 is aligned by adjusting the terminal set-up, while the PC M24 is provided with a diskette containing some MS-DOS commands which set the serial interface to work with the established parameters.

10 PREPROGRAM (1/0)

(Default value = 1).
This function enables the operator to alter the test execution parameters. Hit 1 + ENTER if this funtion is required or hit 0 + ENTER if NOT required (i.e. to run program with the existing default parameters).

11 STOP ERROR (1/0)

With STOP ERROR at 1, the program is interrupted after each error message. At this point, the operator can either continue the test or return to Monitor. When STOP ERROR = 0, the program is not interrupted when error messages are displayed.

Hit 1 + ENTER or 0 + ENTER as required.

12) LOOP ERROR (1/0)

(Default value = 0).
This command cannot be activated with programs inserted prior to Release 8.0.
The command raises the LOOP ERROR flag in the COMMON1 area. Programs use the flag to implement specific loop activities.

Hit 1 + ENTER to implement the function or 0 + ENTER if the functionis not required.

13 DIAGNOSTIC LEV (1..3)

This command establishes the level at which diagnostic messages in output should be pitched. This means essentially that it defines the complexity of data to be fed to the operator if errors are encountered.

- 1 + ENTER selects LEV 1: Only messages giving a brief account of the cause of error are displayed.

- 2 + ENTER selects LEV 2: The TRACEs of N commands (I/O routines) run prior to the error, each with the data (in hexadecimal) relating to the end command response are displayed. The number N is established by the N.TRACE ON ERROR option, described later in this section. The LEV=1 data is then displayed, followed, in some cases, by repair hints. If the error is a "data compare in memory" error, two hexadecimal strings with the contents of the reference buffer and the test buffer, starting from the first incorrect byte and 16 bytes long, are also displayed.

- 3 + ENTER selects LEV 3: In addition to the LEV1 and LEV2 data, the Standard 21 code is also displayed for each error message. A further point to note with DIAGNOSTIC LEV is that the HISTORY feature (see relative section) is only made available to the user when LEV >= 2.

14 CRT CONTROLLER (0..7)

(Default value = 0).
Using this command, the operator selects the keyboard/video controller on which the AUTODIAGNOSTICS are to be run.
The keyboard/video controller is selected by entering a number (0-7) which corresponds to the position of the controller relative to the CPU (i.e. 1 + ENTER to select the controller nearest to the CPU; 2 + ENTER for next nearest controller etc.).

14 EXTENDED MESSAGES 0.1

(Default value = 0)

If using STANDARD WS connected to MUX. or ETS 1010/2010, the EXTENDED MESSAGES facility is available instead of the CRT CONTROLLER facilities.

This facility is used to inhibit the extended service /error messages which are displayed on the video status line.

Hit 1 + ENTER if EXTENDED MESSAGES are required or 0 + ENTER if NOT required.

15 LOOP PROGRAM (1...99999)

With this command, the operator requests a program to be looped a certain number of times (from 1 to 99,999).

Type in the number of program cycles required + ENTER

16 TRACE (1/0 + N.TEST)

Can only be activated if DIAGNOSTIC LEVEL >= 2.
When selected the command field parameters (found in the command registers) are displayed before each I/O operation.

This command permits the operator to control program tracing with respect to the I/O routines.

Hit 1 + ENTER to select the function or 0 + ENTER if function is NOT required.

Hit 00 + ENTER if TRACE is required on all tests or type in the test number + ENTER for the tests on which TRACE is required.

17 DEBUGGING (1/0 + N.TEST)

WARNING:

Data obtained via use of this option is of relevance only to the programmer or design personnel.
For this reason, it must NOT be activated by the end user.

Program design centres use this option to activate parts of codes for program debugging or simulation of software or hardware modules not implemented.

After the program has been issued, this feature is not used, except to look for bugs not discovered in implementation.

Hit 1 + ENTER to impliment DEBUGGING, then either hit 0 + ENTER to implement debugging on all tests or type in the test number on which debugging is required + ENTER.

18 HARD COPY (1/0 + KIND BAUD)

(Default value = 0 i.e. hard copy NOT selected).

Hit 1 + ENTER to select auxiliary printer, then type XXYY + ENTER; where XX = code for the type of message to be displayed (KIND) and YY = code for the transmission rate (BAUD).

- KIND CODES:

. 01 prints HEADING messages only

. 02 prints SERVICE messages only

. 04 prints ERROR messages only

. 20 prints SUMMARY messages only

where:

- HEADING messages are program names and names of tests within the program.

- SERVICE messages are data fed by the program to the operator relating to program progress.

- ERROR messages, give fault details.

- SUMMARY messages are displayed after diagnostic program execution and give a brief account of diagnostic findings in the course of the program.

  If the program is looped, the summary message will be displayed only after the final test run.

Several kinds of messages may be printed simultaneously, producing a code which is the sum of the codes of the various types of message printed. E.g. KIND CODE = 27 = (1+2+4+20): in this case, all four types of message are printed.

- BAUD CODES:

. 00 Transmission speed 50 baud

. 01 " " 110 baud

. 02 " " 300 baud

. 03 " " 600 baud

. 04 " " 1200 baud

. 05 " " 2400 baud

. 06 " " 4800 baud

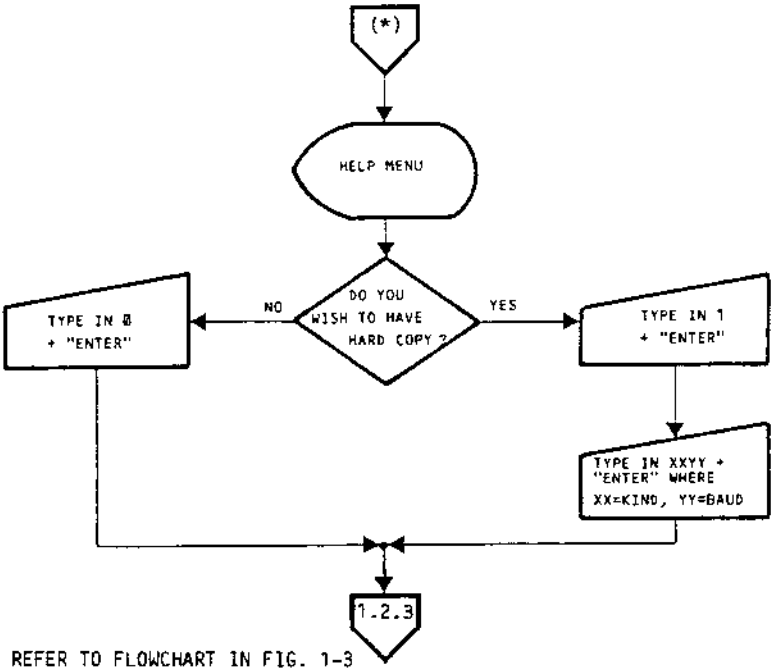
. 07 " " 9600 baud

. 08 " " 19200 baud

. 09 " " 38400 baud

N.B.
On line transmission protocol is as shown below:

- 7 bit
- even parity
- 1 stop bit
- xon xof



(*) REFER TO FLOWCHART IN FIG. 1-3

Fig. 1-18 HARD COPY command procedures

N.B.:

In connection to ETS 1010/2010, this feature is not enabled since the RS 232 channel is occupied by the ETS itself and is not therefore available for the printer. If the option is selected by mistake, the monitor returns automatically to section 1.2.3.

21 WINDOW (0/1)

This command is used to display the summary messages, page by page, with an interval between each page. Hit 1 + ENTER for this feature or 0 + ENTER to SKIP.

Hit "ENTER" to move on to the next video page, after the display of:

--More--

To go back to the program, hit "SKIP" instead.

1.2.3.4 LEVEL TWO MESSAGES

This section is intended for technicians who wish to use level two messages.

Level 2 messages are all further items of information which the DIAGNOSTIC MONITOR can supply in addition to the Level 1 message describing the error cause.

The Level 2 messages are displayed and printed as the operator requires. The Monitor feature commanding display and printing is the "13 DIAGNOSTIC LEVEL", used in combination with "16 TRACE" and/or "20 N.TRACE on ERROR".

The range of possibilities depends on Monitor settings and is summarized in the table below:

		16 TRACE		20 N.TRACE ON ERROR
		1	0	(xx)
	N.TEST=nn	N.TEST=00		
1	Level 1 error messages	Level 1 error messages	Level 1 error messages	Level 1 error messages
13 DIAGNOS. LEV 2	As Lev. 1 + display of I/O routines for test nn and relative parameters + History	As Lev. 1 + display of I/O routines for all tests and relative parameters + History	As Lev. 1 +	As Lev. 1 + display of last xx I/O routines run before each error + parameters + History
3	As Lev. 2 + Standard 21	As Lev. 2 + Standard 21	As Lev. 2 + Stand. 21 +	As Lev. 2 + Standard 21

COMPOSITION OF LEVEL 2 MESSAGES

All Level 2 messages contain a description of an Input/Output Routine.

The following are displayed in order:

- the name of the I/O routine issued
- the contents of the CPU registers with the parameters for the Routine
- the contents of CPU register R7 with the response from the peripheral unit at the end of the Routine, and any associated records.

This information is displayed in the following format:

```
"I/O routine name" Rx=XXXX Ry=YYYY ... RRz=ZZZZ ...
 ...
answer R7=NNNN Rk=KKKK .....
```

Rx and Ry are registers with the parameters for the Routine and XXXX and YYYY, respectively, the contents (idem for double register RRz and ZZZZ). Register R7 contains a code indicating the outcome of the I/O Routine, as well as any other information found in the output record Rk.

For a description of the individual I/O Routines and the contents of the registers, see the "Functional Checks - Input/Output Routines" manual, code no. 4102070 C.

HISTORY FEATURE

The monitor setting for this feature is DIAGNOSTIC LEVEL >= 2.
For all commands issued in diagnostic program execution, the second level message pertaining to the I/O routine is stored in a buffer.
If there are errors, the first level messages will also be stored.
As a result, the buffer will have the history of all commands issued and any errors found in the course of program execution.
When the monitor STOP ERROR setting is 1, each time execution is interrupted because of an error, the program user should give the Monitor command to continue execution. The final section of this cyclic buffer is then displayed on video. The operator can explore the buffer by way of the following commands, entered via the numeric keyboard:

. "8": to have the first part of the buffer displayed

  The top of the buffer is identified by the label:

  ********* HISTORY TOP**********

. "2": to have the last part of the buffer displayed. The label indicating the bottom of the buffer is:

  ********* HISTORY BOTTOM*********

- "1": to have contents scanned one at a time in the "BOTTOM BUFFER" direction.
  In practice, the item immediately following the one currently on video is displayed.

- "7": to have contents scanned one at a time in the "TOP BUFFER" direction.
  The item immediately preceding the one currently on video is displayed.

- "9": to have the entire buffer contents displayed.
  The last named command must only be used if a printer is connected.

- "5": EXIT. Control is returned to the program.

1.2.4 PROGRAM EXECUTION IN DIAGNOSTIC ENVIRONMENT

The program is normally arranged into 2 main sections: the PRE-PROGRAM and MAIN PROGRAM.

The PRE-PROGRAM comprises the interactive part which requires input from the operator and the MAIN-PROGRAM comprises the automatic part which execute the tests and processes the errors (if any).

The programs are generally organised in sub-tests. The sub-tests have titles and each have a test number. The test number and title are shown in the "TABLE OF TEST AND CYCLES displayed at the end of the Pre-program.

The TABLE OF TEST AND CYCLES contains a list of tests and the default TEST SEQUENCE table. This table gives the order in which tests will be run and the number of times each test is to be cycled.

1.2.5 HELP RUN TIME

1.2.5.1 Foreword

Help Run Time is a series of Monitor routines which can be called up, during program execution, after the pre-program phase and before the test itself is activated.

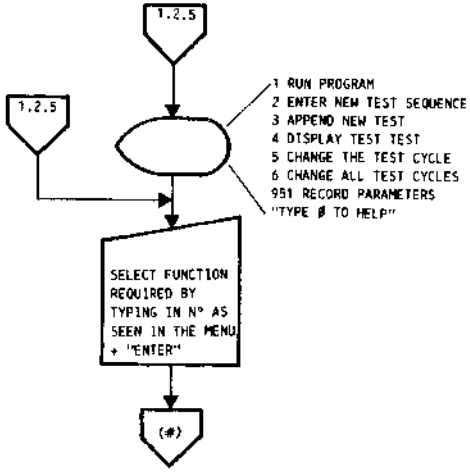
The routines can be used by the operator to modify the TEST SEQUENCE, thus obtaining the best results for the program for each particular context.

Depending on the program being run, MONITOR will display the full menu with 7 items, or a reduced menu of only 5 items. The full menu gives the added possibility of altering the individual test execution sequence. The reduced menu does not offer this feature.

The HELP RUN TIME MENU is called up by hitting "0" and then "ENTER" in response to the`type "0" to help' prompt.

If the number which corresponds to the required funtion listed in the MENU is known then entering this number in responce to the`type "0" to help' prompt will access the appropriate routine without displaying the MENU.

The remainder of this section describes the relative operating procedures for the two types of MENU.



(#) See relative section for function

Fig. 1-4 Help Run Time (full menu) operating procedures

1 run program

This is the start of the test execution phase proper. Once initiated the program will run automatically taking into account the parameters set in the pre-program and in the TABLE OF TEST AND CYCLES.

2 enter new test sequence

The following is displayed:

```
TABLE OF TEST AND CYCLES
    n  ZZZZZZZZ
    :    :   :          WHERE: n = test number
    :    :   :            ZZZZZZ = test title
    n  ZZZZZZZZZ

TEST SEQUENCE
(test number) -(cycles)
    n-y  n-y              n = test number
    n-y  n-y              y = number of cycles

APPEND NEW TEST
(C/R TO END)
 test n cycle = y
 new cycle    = -         type new cycle + ENTER
```

Type new cycle and hit ENTER for each test

3 append new test

Further tests can be added to those currently in the TEST SEQUENCE table.

Type the number of the test to be added + ENTER as indicated on display.

4 display test list

The TABLE OF TESTS AND CYCLES is displayed as already described.

This table give the list of tests in the order in which tests will be run and the number of times each test is to be cycled.

The following symbols in the TABLE OF TESTS AND CYCLES indicate whether tests can be looped or omitted for correct test results.

X = " " (blank): test cannot be omitted
X = "?": test can be omitted
X = "*": test cannot be looped
X = "&": test cannot be looped and cannot be omitted

5 change the test cycle

The operator is requested to enter the number of cycles required per test.

Type in new cycle for test indicated + ENTER

Hit ENTER only if a new cycle is NOT required for a particular test.

6 change all test cycles

A new loop number, applied to all tests, can be set.

Type new cycle number (for all tests) + ENTER

951 record parameters

Parameters set by the operator can be stored in a reserved area of the diagnostic disk (these are the pre-program response, test sequence and loop number parameters).

Hit 951 + ENTER to store the parameters on disk.

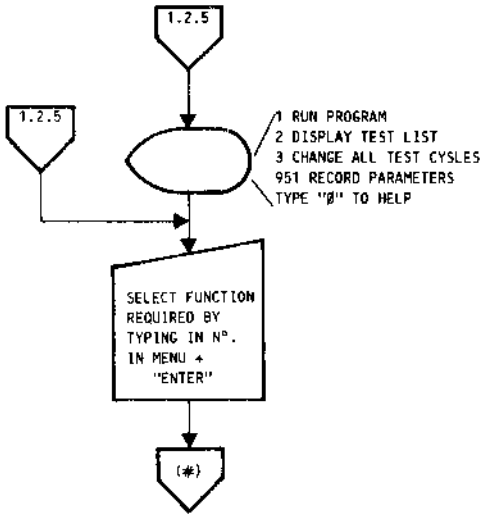
N.B.

1. Before issuing this command, check that the diagnostic disk is correctly installed.

2. After the parameters have been stored, the test is NOT carried out, even on return to the pre-program.

To proceed to test execution, return to MONITOR and re-start the test program (e.g., via the 4 GO command).

1.2.5.3 Help Run Time (reduced menu) operating procedures



(#) See relative section for function

Fig. 1-5 Help Run Time (reduced menu) operating procedures

The reduced version of the Help run time is essentially similar to the full version, minus the "enter new test sequence" and "append new test" features.

The other commands are described in the section on the full Help run time menu.

1.3 INTRODUCTION TO FUNCTIONAL CHECKS PROGRAMS

1.3.1 FOREWORD

Before ANY of the FUNCTIONAL CHECKS programs can be used the AUTODIAGNOSTICS described in section 1.1 must be successfully concluded and the DIAGNOSTIC MONITOR described in section 1.2 correctly installed in SYSTEM RAM.

PROGRAM PURPOSE

To check peripherals and networks as defined in each FUNCTIONAL CHECKS program.

SYSTEM CONFIGURATION

The basic system configuration is given in the introduction section of this manual. Any additional or specific hardware requirements are indicated in the individual programs.

1.3.2 LOADING PROCEDURES

Switch ON and wait for the results of the AUTODIAGNOSTICS. If results are OK, insert disk or tape on the magnetic medium and wait for the DIAGNOSTIC MONITOR to be loaded. When the SYSTEM CONFIGURATION is displayed on the video, note the slot position(s) of board(s) under test (as most programs require this information to be entered in the pre-program) and proceed with the following instructions:

Type ENTER to access the MONITOR and display the MONITOR MASK.

a) To load program:

   1. Type 1XXX + ENTER where XYZ = program code (If code less than 100, X =0; If code less than 10, XY =00).

   OR

   1. Type 1 + ENTER to load the LOAD module.

      When the LOAD module has been loaded, the program code request is displayed on the video.

   2. Type the program code + ENTER to load the program and proceed with the instructions indicated on the video.

b) To access program library:

   1. Type 2 + ENTER to select MAP (PGMS)

   2. Hit ENTER to return to MONITOR (if on last page) or turn page (if NOT on last page).

c) To access MONITOR HELP in order to make use of the facilities detailed in section 1.2.3.

Type 3 + ENTER to go into HELP.

d) To re-run program (only if program has been previously loaded):

Type 4 + ENTER

ERROR MESSAGES

Error indication is provided by either an error message on the video or a coded message on the console or on the video. See DIAGNOSTIC MESSAGES in section 1.1.2. for details on coded messages.

1.3.3 SUMMARY

The manual is divided into 19 chapters.

CHAPTER	SUBJECT(S)
1	AUTODIAGNOSTICS, DIAGNOSTIC MONITOR and INTRODUCTION TO FUNCTIONAL CHECKS PROGRAMS
2	UTILITY SERVICES, ENVIRONMENT ACTIVATOR and DIAGNOSTIC ACTIVATOR
3	SYSTEM RAM and SYSTEM CPU
4	PRINTER/PIN-PAD READER and associated controllers, ENCRIPTION controllers and the M64/M70 console.
5	M60 programs
6	VIDEO-KEYBOARDS
7	WS via MUX and ELB 3683 controllers.
8	Non intelligent line controllers.
9	Intelligent line controllers.
10	MFDU and FDU
11	STC and associated controllers.
12	MTU and associated controllers.
13	HDU 18 MB (XU 5010) and controllers.

CHAPTER	SUBJECT(S) (CONTINUED)
14	HDU 14 MB (XU 5006) and controllers.
15	HDU 60 MB (XU 1700) and controllers.
16	HDU 120 MB (XU1703) and controllers.
17	HDU via ST506 interface and controller.
18	HDU 140 MB via ESDI interface.
19	HDU 275 MB via SMD interface.

2. UTILITY PROGRAMS

2.1 UTILY8: UTILITY PROGRAM

PROGRAM PURPOSE

This program permits the operator to access various utility services in order to display a list of diagnostic programs, display, transfer and/or modify keyboard parameters and contents of physical sectors, and copy whole or part of the diagnostic system.

The program can also be used to add programs on HDUs which already have DCOS installed.

HARDWARE REQUIRED

FDU/MFDU controller, and, as required 2 FDUs or 1 MFDU, or 1 FDU and 1 MFDU, or 2 MFDU, or HDU (with DCOS) and HDU controller.

HDU systems:

PERIPHERAL			CONTROLLER
OPE	(XU5010)	18 MB	G0230 and G0231
FUJITSU	(XU1700/1703)	60/120 MB	G0301 and G0302 (SMD3)
WREN1/2	(XU1707/1709)	27/65 MB	G0363 (ST506)
MICROPOLIS 1325		65 MB	G0363 (ST506)
OPE	(XM5221)	20 MB	G0363 (ST506)
WREN2 DOWNGRATED		40 MB	G0363 (ST506)
MICROPOLIS 1323/A DOWNGRATED		40 MB	G0363 (ST506)
HDU	(XU5006)	14 MB	G0299 and DTC-510B (SASI) or G0363 (ST506)
WREN3		140 MB	G0404 and G0405 (ESDI)
MICROPOLIS 1353/1355		70/140 MB	G0404 and G0405 (ESDI)
FUJITSU	M2246E	140 MB	G0404 and G0405 (ESDI)
PATRIOT	9720 EMD	275 MB	G0301 and G0302 (SMD3)

Other systems:

PERIPHERAL			CONTROLLER
FDU	(XG6030)	1 MB	G0280/D
MFDU	(XU4301)	320 KB	G0280/E
MFDU	(XU4305)	1 MB	G0280/D

LOADING PROCEDURES

Refer to section 1.3.2.

2.1.1 PROGRAM DESCRIPTION

DIAGNOSTIC DISK CATALOGUE

This utility displays the list of diagnostic programs, release number, issue date, number of sectors occupied by each program, first track and sector number of each program and the last track and sector of each program.

KEYBOARD TABLES SERVICE

This facility permits the keyboard tables in the TABK file to be displayed and, if required, permits a different keyboard table to be installed on the disk in order to modify the keyboard funtions.

The keyboard table can be transferred to other disk units.

DISK UNIT TO KEYBOARD (ASCII)

This facility permit the contents of physical sectors to be displayed (in ASCII code) and modified.

PHYSICAL BLOCK TRANSFER

This facility permits the physical blocks to be transferred from FDUs or MFDUs to other FDUs/MFDUs.

FDU PROGRAMS APPEND TO HDU SYS

This facility permits FDU diagnostic programs to be appended onto a list of diagnostic programs on HDUs which already have DCOS installed.

DISK UNIT TO KEYBOARD (HEX.)

This facility permits the contents of physical sectors to be displayed (in HEX code) and modified.

DIAGNOSTIC SYSTEM TRANSFER

This facility permits the DIAGNOSTIC SYSTEM (BOOTSTRAP, MONITOR and selected DIAGNOSTIC PROGRAMS) to be copied from FDUs or MFDUs to other FDUs/MFDUs.

2.1.2 ERROR MESSAGES

I/O ERROR ON UNIT X (S0 = RETRY S2 = EXIT); X = unit number

Try to re-issue the I/O command by hitting S0 or hit S2 to exit program and re-load the program. If LED L2 is lit hit clear key. If fault persists verify/change magnetic medium and associated controller(s).

2.2 LDHSE2: HDU ENVIRONMENT ACTIVATOR LOAD PROGRAM - FOR STANDARD WS

PROGRAM PURPOSE

To load the environment activator onto the HDU from FDU, MFDU (1MB), STC or MTU using a standard WS.

HARDWARE REQUIRED

HDU system, and one of the following systems: FDU and FDU controller board, MFDU (1MB) and MFDU controller board, STC and STC controller board or MTU and MTU controller board.

HDU systems:

HDU	CONTROLLER
OPE 18MB (XU5010)	G0230 andG0231
FUJITSU (XU1700/1703)	G0301 and G0302 (SMD3)
WREN1/2 (XU1707/1709)	G0363 (ST506)
MICROPOLIS 1325	G0363 (ST506)
HD 14MB (XU5006)	G0363 (ST506) OR G0363/G0299 and DTC-510B (SASI)

Other systems:

PERIPHERAL	CONTROLLER
STC (XU1120)	G0200/X or B and G0201/B
STC (XU1130)	G0200B and G0342
FDU (XU6030)	G0280D
MFDU 1MB (XU4305)	G0280D
MTU (XU1705)	G0278B

NOTE

The HDU may already be equipped with an Operating System.

LOADING PROCEDURES

Refer to section 1.3.2.

2.2.1 PROGRAM DESCRIPTION

ENVIRONMENT ACTIVATOR LOADING

The program permits the environment activator to be installed on a selected HDU or for the resident activator to be disabled. After loading the activator (on the first seven sectors of the HDU, starting from sector 0, cylinder 0, head 0), the operating environment can be selected.

ENVIRONMENT SELECTION

The diagnostic environment is selected by entering 5 then 0. If the code is NOT entered within 5 seconds after the message "SEL (R:XX)" starts to blink, the first active operating system resident on the HDU is loaded by default. If there are no operating systems on disk or if it is not possible to load the diagnostic system, the code "E" will be displayed on the WS video.

2.2.2 ERROR MESSAGES

Verify/change magnetic medium and associated controller(s) as appropriate.

- ABNORMAL HARD DISK UNIT
- NO HDU AVAILABLE IN SYSTEM
- ERROR - PROGRAM ABORT

2.3 LDHMU7: HDU ENVIRONMENT ACTIVATOR LOAD PROGRAM - FOR WS OR M24, VT100

PROGRAM PURPOSE R 4,1

To load the environment activator onto the HDU from STC, FDU, MFDU (1MB) or MTU using:

- standard WS
- WS, M24 or VT100 connected via MUX
- M24 or VT100 connected to the RS232 port on the UC board.

HARDWARE REQUIRED

HDU system, and one of the following systems: FDU and FDU controller board, MFDU(1MB) and MFDU controller board, STC and STC controller board or MTU and MTU controller board.

HDU systems:

PERIPHERAL			CONTROLLER
OPE	(XU5010)	18 MB	G0230 and G0231
FUJITSU	(XU1700/1703)	60/120 MB	G0301 and G0302 (SMD3)
WREN1/2	(XU1707/1709)	27/65 MB	G0363 (ST506)
MICROPOLIS 1325		65 MB	G0363 (ST506)
OPE	(XM5221)	20 MB	G0363 (ST506)
WREN2 DOWNGRATED		40 MB	G0363 (ST506)
MICROPOLIS 1323/A DOWNGRADED		40 MB	G0363 (ST506)
HDU	(XU5006)	14 MB	G0299 and DTC-510B (SASI) or G0363 (ST506)
WREN3		140 MB	G0404 and G0405 (ESDI)
MICROPOLIS 1353/1355		70/140 MB	G0404 and G0405 (ESDI)
FUJITSU	M2246E	140 MB	G0404 and G0405 (ESDI)
PATRIOT	9720 EMD	275 MB	G0301 and G0302 (SMD3)

Other systems:

PERIPHERAL			CONTROLLER
FDU	(XG6030)	1 MB	G0280/D
MFDU	(XU4305)	1 MB	G0280/D
STC	(XU1120)	20 MB	G0200/B and G0201/B
STC	(XU1130)	20 MB	G0200/B and G0342
STC	(XU4950)	45/60 MB	G0417 and G0418
MTU	(XU1705)	40 MB	G0278/B

LOADING PROCEDURES

Refer to section 1.3.2

2.3.1 TEST DESCRIPTION

Refer to section 2.2.1 for description. The environment activator in this case, however, is also located in the user area as pointed by the Lable SWBOOT.

2.3.2 ERROR MESSAGES

Refer to section 2.2.2.

2.4 LDHS33: HDU ENVIRONMENT ACTIVATOR LOADING PROGRAM - FOR ETS WS

PROGRAM PURPOSE

To load the environment activator onto the HDU from STC, FDU, MFDU (1MB) or MTU using WS type ETS.

HARDWARE REQUIRED

HDU system, and one of the following systems: FDU and FDU controller board, MFDU(1MB) and MFDU controller board, STC and STC controller board or MTU and MTU controller board.

HDU systems:

HDU	CONTROLLER
OPE 18MB (XU5010)	G0230 andG0231
FUJITSU (XU1700/1703)	G0301 and G0302 (SMD3)
WREN1/2 (XU1707/1709)	G0363 (ST506)
MICROPOLIS 1325	G0363 (ST506)
HD 14MB (XU5006)	G0363 (ST506) OR G0363/G0299 and DTC-510B (SASI)

Other systems:

PERIPHERAL	CONTROLLER
STC (XU1120)	G0200/X or B and G0201/B
STC (XU1130)	G0200B and G0342
FDU (XU6030)	G0280D
MFDU 1MB (XU4305)	G0280D
MTU (XU1705)	G0278B

LOADING PROCEDURES

Refer to section 1.3.2.

2.4.1 PROGRAM DESCRIPTION

Refer to section 2.2.1 of the LDHSE2 program.

2.4.2 ERROR MESSAGES

Refer to section 2.2.2 of the LDHSE2 program.

2.5 SYSINB: COPY PROGRAMS FROM STC, FDU, MFDU(1MB) OR MTU TO HDU

PROGRAM PURPOSE

To copy the diagnostic monitor and the test programs from FDU, MFDU (1MB), STC or MTU onto HDU.

HARDWARE REQUIRED

CPU board, RAM board, HDU system, and one of the following systems: FDU and FDU controller board, MFDU(1MB) and MFDU controller board, STC and STC controller board or MTU and MTU controller board.

HDU systems:

PERIPHERAL			CONTROLLER
OPE	(XU5010)	18 MB	G0230 and G0231
FUJITSU	(XU1700/1703)	60/120 MB	G0301 and G0302 (SMD3)
WREN1/2	(XU1707/1709)	27/65 MB	G0363 (ST506)
MICROPOLIS 1325		65 MB	G0363 (ST506)
OPE	(XM5221)	20 MB	G0363 (ST506)
WREN2 DOWNGRATED		40 MB	G0363 (ST506)
MICROPOLIS 1323/A DOWNGRATED		40 MB	G0363 (ST506)
HDU	(XU5006)	14 MB	G0299 and DTC-510B (SASI) or G0363 (ST506)
WREN3		140 MB	G0404 and G0405 (ESDI)
MICROPOLIS 1353/1355		70/140 MB	G0404 and G0405 (ESDI)
FUJITSU	M2246E	140 MB	G0404 and G0405 (ESDI)

Other systems:

PERIPHERAL			CONTROLLER
FDU	(XG6030)	1 MB	G0280/D
MFDU	(XU4305)	1 MB	G0280/D
STC	(XU1120)	20 MB	G0200/B and G0201/B
STC	(XU1130)	20 MB	G0200/B and G0342
STC	(XU4950)	45/60 MB	G0417 and G0418
MTU	(XU1705)	40 MB	G0278/B

NOTE:

The diagnostic environment and IPL must be installed from the same disk unit.

WARNING:

If the diagnostic environment is being re-installed, the operator should first ensure that the space reserved on the HDU is large enough for the new diagnostic release.

LOADING PROCEDURES

Refer to section 1.3.2.

2.5.1 PROGRAM DESCRIPTION

The program first performs a check to ensure that the required controllers are present. The HDU is then initialised and the diagnostic programs copied onto the HDU.

2.5.2 ERROR MESSAGES

All blocking errors, in addition to the string identifying the type of error, are accompanied by the following:

- SORRY
- BUT WE MUST RETURN CONTROL TO MONITOR
- HIT "ENTER" PLEASE

When this message appears, the operator should first hit "ENTER" to return to the diagnostic monitor and then investigate the error.

ERROR LIST

The errors which may be encountered listed below. Unless otherwise indicated verify/change magnetic medium and associated controller(s).

- ****** BAD MAGIC NUMBER ****** (a non-existent PU has been selected. Not a hard error)
- WRONG OPERATION,HDU CONTROLLER ALREADY INITIALIZED (the HDU itself has tried to run the program)
- HDU CONTROLLER SYSTEM ABSENT
- WRONG HDU INITIALIZATION (HDU controller initialization failure). A code identifying the type of error is displayed:
  - 1 = controller error
  - 2 = peripheral unit error
- WRONG STC INITIALIZATION = (STC controller initialization failure. A code identifying the type of error is displayed:
  - 1 = controller error
  - 8 = magnetic medium missing
- HDU KO OR BAD CONNECTION
- INSUFFICIENT SPACE ON HDU
- SUBSYSTEM LABEL IDENTIFIER ABSENT

- ALL O.S. DESCRIPTOR BUSY (the OS descriptors have been initialized)

- STC CONTROLLER ERROR (error in transfer of data from STC to HDU, caused by STC. A code identifying the type of error is displayed:

  . 1 = controller error

  . 2 = peripheral unit error

  . 4 = medium error

  . 8 = magnetic medium missing

  . 10 = end of track

  . 40 = tape mark

- HDU CONTROLLER ERROR = data receive error, caused by HDU. A code specifying the type of error is displayed:

  . 1 = controller error

  . 2 = peripheral unit error

  . 4 = medium error

- FDU MODE ASSIGNMENT (incorrect FDU or MFDU work mode (128/256 byte per sector))

- FDU CONTROLLER ERROR (error in transfer of data from FDU or MFDU to HDU, caused by FDU).

- STC ERROR : INOP (operator intervention while STC in operation)

- STC ERROR : BUSY OR ADDRESS (channel busy or address is incorrect)

- RECOVERY ERROR IN WRITING HDU (write error during recovery procedure issue)

- MTU : TIME OUT ERROR (end interrupt has not come through in initialization, rewind or read operations. Controller is at fault)

- MTU UP ERROR (error in initialization - incorrect jumper on controller of unit connected or the unit is off line. The error is signalled by the failure of the ON LINE LED to illuminate).

- MTU CONTROLLER ERROR (MTU controller faulty).

- ENVIRONMENT LENGTH IS SMALLER THAN IPL UNIT CONTENTS (the total area available on HDU is not large enough: in cases where the diagnostic environment program has been loaded already)

- SELECTED LENGTH IS SMALLER THAN IPL UNIT CONTENTS (the area selected is too small)

2.6 HDSCT9: INSTALL DIAGNOSTIC ENVIRONMENT ON STC FROM HDU

PROGRAM PURPOSE

This program installs the diagnostic environment resident on the HDU onto the STC.

HARDWARE REQUIRED

HDU system and STC system.

HDU systems:

PERIPHERAL			CONTROLLER
OPE	(XU5010)	18 MB	G0230 and G0231
FUJITSU	(XU1700/1703)	60/120 MB	G0301 and G0302 (SMD3)
WREN1/2	(XU1707/1709)	27/65 MB	G0363 (ST506)
MICROPOLIS 1325		65 MB	G0363 (ST506)
OPE	(XM5221)	20 MB	G0363 (ST506)
WREN2 DOWNGRATED		40 MB	G0363 (ST506)
MICROPOLIS 1323/A DOWNGRATED		40 MB	G0363 (ST506)
HDU	(XU5006)	14 MB	G0299 and DTC-5108 (SASI) or G0363 (ST506)
WREN3		140 MB	G0404 and G0405 (ESDI)
MICROPOLIS 1353/1355		70/140 MB	G0404 and G0405 (ESDI)
FUJITSU	M2246E	140 MB	G0404 and G0405 (ESDI)

STC systems:

PERIPHERAL			CONTROLLER
STC	(XU1120)	20 MB	G0200/B and G0201/B
STC	(XU1130)	20 MB	G0200/B and G0342

INTRODUCTORY NOTES

The diagnostic environment can only be installed on the STC using the same HDU from which the IPL was made.

As no certification or tests of the units concerned in the transfer are provided for in the program, the units must be checked beforehand to ensure that they are in perfect working order. This is done to prevent breakdowns or program interruptions.

The STC must be dedicated exclusively to execution of this program as all its previous contents are destroyed.

LOADING PROCEDURES

Refer to section 1.3.2.

2.6.1 TEST DESCRIPTION

The program consists of a single operation, which can be divided into 3 separate stages:

1. IPL VERIFY, STC INIT RUNNING
   This checks that IPL has not been made from STC, FDU or MTU.
   The STC controller is then initialized and the tape pre-conditioned.

2. STC ERASE RUNNING
   All four tape tracks are erased.

3. HDU-STC TRANSFER RUNNING
   All the STAND ALONE diagnostic modules on the HDU (Bootstrap, Monitor, Programs, Library) are transferred on to the Streaming Cartridge Tape.
   The diagnostic system is stored on STC track 0 and the program library on the first blocks of track 2.
   The tape is completely rewound when storage has been completed.

N.B.
When program execution is finished, the system should be set to "Secondary" position and reset in order to perform IPL from the STC.

2.6.2 ERROR MESSAGES

Verify/change magnetic medium and associated controller(s) as appropriate.

- ERROR: IPL NOT EXECUTED FROM HDU = the diagnostic transfer program has not been loaded in memory by the HDU but by the FDU or STC
- STC CONTROLLER FAULT (absent: control is returned to Monitor)
- HDU CONTROLLER ERROR (in HDU initialization: control is returned to Monitor)
- STC CONTROLLER ERROR (in STC initialization: control is returned to Monitor)
- CARTRIDGE ABSENT ERROR (no cartridge: control is returned to Monitor)
- STC ERROR:WRITE PROTECT (cartridge is write protected: control is returned to Monitor)
- STC ERROR:BAD CONTROL AFTER WRITING (read control error after a write: program control returns to Monitor)
- STC ERROR:ALREADY RECORDED CARTRIDGE (already recorded or not erased: program control returns to Monitor)
- STC ERROR:ABORT (program control returns to Monitor)
- STC ERROR:BAD WRITING OR HARD ERROR (in STC write phase: program control returns to Monitor)

- STC ERROR:INOP (operator intervention on STC, e.g. has removed cartridge: program control returns to Monitor)

- STC ERROR:BUSY OR ADDRESS (channel busy or incorrect address: program control returns to Monitor)

- ODD PROGRAM LENGTH ** PROGRAM ABORT ** = Programs of lengths not multiples of 512 Kbytes and not uniform

When any of these messages appears, the program returns automatically to Monitor control.

2.7 HDNTU7: INSTALL DIAGNOSTIC ENVIRONMENT FROM HDU TO MTU

PROGRAM PURPOSE

This program installs the diagnostic environment resident on the HDU onto the MTU

HARDWARE REQUIRED

HDU system, and MTU system.

HDU systems:

PERIPHERAL			CONTROLLER
OPE	(XU5010)	18 MB	G0230 and G0231
FUJITSU	(XU1700/1703)	60/120 MB	G0301 and G0302 (SMD3)
WREN1/2	(XU1707/1709)	27/65 MB	G0363 (ST506)
MICROPOLIS 1325		65 MB	G0363 (ST506)
OPE	(XM5221)	20 MB	G0363 (ST506)
WREN2 DOWNGRATED		40 MB	G0363 (ST506)
MICROPOLIS 1323/A DOWNGRATED		40 MB	G0363 (ST506)
HDU	(XU5006)	14 MB	G0299 and DTC-510B (SASI) or G0363 (ST506)
WREN3		140 MB	G0404 and G0405 (ESDI)
MICROPOLIS 1353/1355		70/140 MB	G0404 and G0405 (ESDI)
FUJITSU	M2246E	140 MB	G0404 and G0405 (ESDI)
PATRIOT	9720 EMD	275 MB	G0301 and G0302 (SMD3)

MTU system:

PERIPHERAL			CONTROLLER
MTU	(XU1705)	40 MB	G0278/B

INTRODUCTORY NOTES

The diagnostic environment can only be installed on the MTU using the same HDU from which the IPL was made.

As no certification or tests of the units concerned in the transfer is provided for in the program, the units must be checked beforehand to ensure that they are in perfect working order. This is done to prevent breakdowns or program interruptions.

Also the MTU selected must have its LOAD/REWIND, ON LINE and WRT ON TEST key LEDs permanently on.

The magnetic tape of the MTU must be completely dedicated to the transfer operation and have sufficient capacity to receive the HDU diagnostic system.

LOADING PROCEDURES

Refer to section 1.3.2.

2.7.1 TEST DESCRIPTION

The program consists of a single operation, the transfer of the diagnostic system from HDU to MTU, which can be considered as being in 6 distinct phases:

1. CHECK IPL, MTU INIT RUNNING
   This checks that the IPL has not been made from STC, FDU or MTU; the MTU controller initialization is also carried out.

2. MTU REWIND
   The tape is completely rewound.

3. MTU ERASE RUNNING
   The whole tape is erased.

4. MTU REWIND
   The tape is completely rewound.

5. HDU-MTU TRANSFER RUNNING
   All the HDU STAND ALONE diagnostic modules (Bootstrap, Monitor, Programs, Library) are transferred on to magnetic tape.

6. MTU REWIND
   The tape is completely rewound.

N.B.
Following program execution, the system must be switched to the "secondary" position and then reset in preparation for IPL from the MTU.

2.7.2 ERROR MESSAGES

Verify/change the HDU/MTU and associated controller(s) as appropriate.

- ERROR: IPL NOT EXECUTED FROM HDU :
  the STAND ALONE DIAGNOSTIC transfer program has not been loaded into memory from the HDU, but from STC, MTU or FDU. Control is returned to Monitor.

- MTU CONTROLLER FAULT :
  MTU controller is missing. Control is returned to Monitor.

- HDU CONTROLLER ERROR :
  error in HDU initialization. Control is returned to Monitor.

- MTU CONTROLLER ERROR :
  error in MTU initialization (controller faulty). Control is returned to Monitor.

- MTU ERROR :
  error in MTU initialization (incorrect jumper connection on unit or unit OFF LINE signalled through failure of ON LINE LED to come on or through insufficient tape capacity). Control is returned to Monitor.

- MAGNETIC TAPE ERROR :
  the tape is write protected (no rear red ring on tape). This will also be signalled by the failure of the WRT EN TEST LED on the console to come on. Program control returns to Monitor.

- TIME OUT HDU :
  interrupt does not occur in HDU SMD read (controller fault or program error). Program control returns to Monitor.

- TIME OUT MTU :
  interrupt does not occur in MTU initialization, rewind, erase or write operations (cause may be controller fault, program error or insufficient tape capacity). Program control returns to Monitor.

- END OF TAPE the tape has a capacity less than the value specified in the DCOS system installed on HDU.

2.8 HDUFD7: INSTALL DIAGNOSTIC ENVIRONMENT FROM HDU TO FDU/MFDU

PROGRAM PURPOSE

This program installs the diagnostic environment resident on the HDU onto the FDU or MFDU.

HARDWARE REQUIRED

HDU system and FDU or MFDU system.

HDU systems:

PERIPHERAL			CONTROLLER
OPE	(XU5010)	18 MB	G0230 and G0231
FUJITSU	(XU1700/1703)	60/120 MB	G0301 and G0302 (SMD3)
WREN1/2	(XU1707/1709)	27/65 MB	G0363 (ST506)
MICROPOLIS 1325		65 MB	G0363 (ST506)
OPE	(XM5221)	20 MB	G0363 (ST506)
WREN2 DOWNGRATED		40 MB	G0363 (ST506)
MICROPOLIS 1323/A DOWNGRATED		40 MB	G0363 (ST506)
HDU	(XU5006)	14 MB	G0299 and DTC-510B (SASI) or G0363 (ST506)
WREN3		140 MB	G0404 and G0405 (ESDI)
MICROPOLIS 1353/1355		70/140 MB	G0404 and G0405 (ESDI)
FUJITSU	M2246E	140 MB	G0404 and G0405 (ESDI)
PATRIOT	9720 EMD	275 MB	G0301 and G0302 (SMD3)

Other systems:

PERIPHERAL			CONTROLLER
FDU	(XG6030)	1 MB	G0280/D
MFDU	(XU4301)	320 KB	G0280/E
MFDU	(XU4305)	1 MB	G0280/D

INTRODUCTORY NOTES

The diagnostic system can only be installed on FDU by using the same HDU that was used for IPL.

As no certification or tests of the units concerned in the transfer is provided for in the program, the units must be checked beforehand to ensure that they are in perfect working order. This is done to prevent breakdowns or program interruptions.

NOTE

The HDU resident library must be no more than 16 sectors long, making a library of 204 programs. The "target" floppy disk should be formatted according to existing standards. Only 256 bytes per sector, double sided, double density MFM disks may be used.

LOADING PROCEDURES

Refer to section 1.3.2.

2.8.1 TEST DESCRIPTION

The program consists of two separate operations:

1. The first is the transfer of the HDU diagnostic system and some or all of the programs in the HDU library to the Floppy disk.

2. In the second, all or some of the programs in the HDU library are "appended" on to the floppy disk (the programs are tagged on after the diagnostic system and library already on the floppy disk).

The operations are carried out depending on the response to the question

SCRATCH OR APPEND ON FLEX-DISK?

asked in the pre-program.

Blocks 104 sectors long at most are transferred consecutively to make the duplicate copy. After they are written, the sectors are read and compared.

2.8.2 ERROR MESSAGES

All errors, regardless of type, are accompanied by the following message:

```
I/O ERROR ON FLOPPY DISK  UNIT
 (PRESS 0 + ENT = RETRY ; 1 + ENT  = RESET)
```

0 + ENTER is pressed to retry program or 1 + ENTER is pressed to return to the start of the program and then 1 + ENTER to return to MONITOR.

If fault persists Verify/change the magnetic medium and associated controller(s).

3.1 UC3003: UC036/UC051 CPU (WITHOUT GATE ARRAY) TEST PROGRAM.

PROGRAM PURPOSE

To test the CPU.

HARDWARE REQUIRED

UC036/UC051 CPU board, RAM board, floppy/mini-floppy controller.

PRELIMINARY OPERATIONS

If the RS232 serial interface lines are to be tested fit plug on the CPU serial 1/0 connector with the following connections made:

Pin A linked to Pin 1	Pin D linked to Pin 4
Pin B linked to Pin 2	Pin E linked to Pin 5
Pin C linked to Pin 3	

CAUTION:

The system printer should not be connected during tests.

LOADING PROCEDURE

Refer to section 1.3.2

3.1.1 TEST DESCRIPTION

The function of each of the tests available is described below:

1. **TRAP REQUEST TEST**

   Checks the generation of the trap request by the MMU and the transitional states of signal DIMEN. All the possible violations of memory are simulated and the MMU checked for correct generation of corresponding trap signal.

2. **VIENO SIGNAL TEST**

   Checks that the set and reset of the VIENO signal (level 2 vectored interrupt) is correct.

3. **TIMER TEST**

Checks the timer circuits as follows:
counter 0, channel 0 in "rate generator" mode; counter 1, channel 1 in "interrupt on terminal count" mode using the first free vector to test the vectored interrupt; counter 2, channel 2 in "square wave rate generator" mode.

4. **ACIA TEST**

Checks the ACIA as follows:

- runs a self-diagnostic test in which the six service signals are checked (only if the external plug is in place),
- runs a polling sequence test using the external loop (if plug is in place) or internal loop (if plug is not in place) for TxD and RxD signals,
- runs a transmission test using the external or internal loop depending whether the loop plug is in place and with the TX/RX interrupt status as follows:
  - Tx enabled and Rx disabled,
  - Tx disabled and Rx enabled,
  - Tx and Rx both enabled,

5. **NON-VECTORED INTERRUPT TEST**

Checks the non-vectored interrupts and associated circuits, in particular tests the input port from which the cause of the interrupt and mask status is read and also the interrupts generated by signals NV1, NV2, NV3 and NV4.

6. **VECTORED INTERRUPT TEST**

Tests the vectored interrupts and registers for storing the vectors by generating a number of vectors using channel 1 of the timer and the ACIA.

7. **ROM TEST**

Checks the CRC contained in the ROM.

8. **EAROM TEST**

Tests the EAROM for shorts in data and address fields and then performs a modified version of the Abraham test.

3.1.2 ERROR AND SERVICE MESSAGES

TRAP REQUEST TEST

- **VIOL./INST TYPE REG. FLAGS FAULT**
  Error in the violation/instruction register flags

- **VIOL./INST TYPE REG. FAULT**
  Error in the violation/instruction register

- **VIOL./INST SEG. NUM. REG. FAULT**
  Error in the violation/intruction segment number register

- **VIOL./INST OFF. REG FAULT**
  Error in the violation/instuction offset register

- **RDV TRAP NOT OCCURRED**
  The Read only Violation trap was not generated

- **SYSV TRAP NOT OCCURRED**
  The System Violation trap was not generated

- **SLV TRAP NOT OCCURRED**
  The System Length Violation trap was not generated

- **CPUIV TRAP NOT OCCURRED**
  The CPU-Inhibit Violation trap was not generated

- **EXCV TRAP NOT OCCURRED**
  The Execute Only Violation trap was not generated

- **PWW TRAP NOT OCCURRED**
  The Primary Write Warning trap was not generated

- **SWW TRAP NOT OCCURRED**
  The Secondary Write Warning trap was not generated

- **BUS CYCLE STATUS REG. FAULT**

- **FATAL CONDITION FAULT**
  A trap was generated even though no bit was set in the violation type register

- **FATAL FLAG STUCK AT 0**
  The FATL (fatal condition) bit is stuck at zero

- **DISABLE/ENABLE INHIBITION MEMORY FAULT**
  The DIMEN signal does not disable/enable the memory

VIENO SIGNAL TEST

- **VIENO STUCK AT 1/0**

TIMER TEST

- **COUNTER 0/2 FAULT**
  Error in channel 0/2 of the timer

- **COUNTER 1 INTERRUPT FAULTING**
  The interrupt for channel 1 was not generated

- **LATCH OUTPUT CNT1 FAULT**
  Error in the output latch

ACIA TEST

- **SIGNAL P01/2/3 (STUCK AT 1/0) OR LATCH FAULT**
  Error in signals P01, P02 or P03 (stuck at 1/0) or in the associated latch

- **TIME-OUT ERROR ON TX/RX READY**
  Time-out error with the transmit/receive register empty

- **STATUS REGISTER FAULT**

- **DOUBLE BUFFERING FAULT**

- **ERROR FLAGS STUCK AT 0**

- **ERROR FLAGS FAULT (STUCK AT 1)**

- **FRAMING/OVERRUN/PARITY ERROR**

- **WRONG DATA RECIVED**

- **TIME-OUT ERROR ON LAST TX DATA**

- **TX REG. FULL AND RX REG. EMPTY**

- **NV1/2/3/4 & ENx: WROTE 1/0 READ 0/1**

NON-VECTORED INTERRUPT TEST

- **INTERRUPT NV1/2/3/4 FAULT**
  The non-vectored interrupt NV1, NV2, NV3 or NV4 was not generated

- **NV1/2/3/4 INTERRUPT MASK FAULT**
  The non-vectored interrupt NV1, NV2, NV3 or NV4 was generated even though it was masked

- **CONCURRENT INTERRUPT FAULT**
  Non-vectored interrupts (set simultaneously) not generated.

VECTORED INTERRUPT TEST

- **NO TIMER INTERRUPT**

- **BAD VECTOR TIMER/ACIA INTERRUPT**

EAROM TEST

- SHORT DATA/ADDRESS ERROR
- FUNCTIONAL ERROR
- LOW/HIGH BANK FAULT
- BANK FAULT -(OR 'ROM SIZE'/'UC TYPE WRONG')

3.2 UC6304: UC042/UC042A CPU (WITH GATE ARRAY) TEST PROGRAM.

PROGRAM PURPOSE

To test the CPU.

HARDWARE REQUIRED

UC042 or UC042A CPU board, RAM board, floppy/mini-floppy disk controller.

PRELIMINARY OPERATIONS

If the RS232 serial interface lines are to be tested fit plug on the CPU serial I/O connector with the following connections made:

Pin A linked to Pin 1	Pin D linked to Pin 4
Pin B linked to Pin 2	Pin E linked to Pin 5
Pin C linked to Pin 3	

CAUTION:

The system printer should not be connected during tests.

LOADING PROCEDURE

Refer to section 1.3.2

3.2.1 TEST DESCRIPTION

Refer to the corresponding section (3.1.1) of the UC3003 program.

3.2.2 ERROR AND SERVICE MESSAGES

Refer to the corresponding section (3.1.2) of the UC3003 program.

3.3 UCV305: CPU FUNCTIONAL CHECKS PROGRAM

PROGRAM PURPOSE

This program is designed to test the UC048 CPU or the UC070 CPU.

HARDWARE REQUIRED

UC048/UC070 CPU board and loop plug.

PRELIMINARY OPERATIONS

If the RS232 serial interface lines are to be tested fit plug on the CPU serial I/O connector with the following connections made:

Pin A linked to pin 1
Pin B linked to pin 2
Pin C linked to pin 3
Pin D linked to pin 4
Pin E linked to pin 5

LOADING PROCEDURES

Refer to section 1.3.2.

3.3.1 TEST DESCRIPTION

Tests 1-8 in this program are the same as tests 1-8 in the UC3003 program (section 3.1.1) except that VIENO SIGNAL TEST becomes MASTO AND VIENO SIGNAL TEST; set and reset of the MASTO signal is also checked.

9. DIP-SWITCHES TEST

The operator can select this test in when setting the parameters. The test reads and displays on the monitor the status of the four DIP-switches present on the CPU board.

10. RESET GENERATION TEST

Like the previous test, this test can be selected when the test parameters are being set, and is controlled by the operator. It consists in generating a hardware reset which reinitializes the whole system (except the CPU).
NOTE: The system must be reset again at the end of this test.

3.3.2 ERROR MESSAGES

Refer to corresponding section (3.1.2) of UC3003 program; the following two messages occur during the MASTO AND VIENO SIGNALS TEST.

- MASTO STUCK AT 1
- MASTO STUCK AT 0

3.4 UCY807: CENTRAL UNIT BOARD UC0 71 TEST PROGRAM

PROGRAM PURPOSE

The purpose of the program is to perform a hardware test of the Central Units in the system, the Bus Arbiter and the Watch-dog logic.

HARDWARE REQUIRED

UC071 board (up to 3 boards may be connected).

PRESETTINGS

For the serial interface test, where the UC071 CPU is connected to the console via the J122 connector, a plug for the hardware loop must be placed on the console J042 connector with the pins connected as shown below:

```
Pin 02 <---> Pin 03
Pin 04 <---> Pin 08
Pin 04 <---> Pin 05
Pin 06 <---> Pin 07
```

In special cases the serial channels may be closed by placing a loop plug on each CPU with connections made as shown below. However the UC071 CPU must then be connected via the console J049 connector and the J122 connector left disconnected.

```
Pin A <---> Pin 1          Pin D <---> Pin 4
Pin B <---> Pin 2          Pin E <---> Pin 5
Pin C <---> Pin 3
```

LOADING PROCEDURES

Refer to section 1.3.2.

3.4.1 TEST DESCRIPTION

1. **SLOT TEST**

   This test checks that the TCBs (both MASTER and SLAVE) are in the position selected by the operator.

2. **MMU TEST**

   This test is performed on MMU1 (defined by address %FC) and on MMU2 (address %FA) as follows:

STEP 1: Saves the contents of MMU1 and then enables both MMUs in translate mode. Then sets the MMU2 Upper Range Select (URS) flag to 1 and checks the status of the 2 MMUs.

Checks the operation of URS flag using MM2 (segments %40 to %7F) to address RAM segment %21.

STEP 2: Writes data ranging from %00 to %FF on 64 registers of MMU2 (each of 4 bytes) and verifies data written after each write.
Then writes 0 (16 bits at a time) on all bits of the same registers and verifies the data written.
Performs a marching 1 test where the data written is changed so that a bit set to 1 moves from left to right and at each change the data written is checked.
Sets the same bits to 1, verifies the result then performs a marching 0 test.

STEP 3: Calculates the step required to incrementally check the available physical RAM.

STEP 4: Uses the physical RAM addresses obtained from the step 3 calculation as Base Addresses so that the 64 MMU2 registers accesses an 8K RAM area.

STEP 5: Uses the %FF00 (CRT dual port RAM) address obtained from an MMU1 register as a Base Address to access the 64 MMU2 registers.

STEP 6: Copies the contents of MMU1 onto MMU2, setting URS flag to 0 on MMU2 and 1 on MMU1.

- STEPS 12 THROUGHT TO 15:

These tests correspond to tests 2 to 5 respectively except that MMU2 used instead of MMU1.

STEP 20 Resets initial conditions on MMU1 and MMU2 and returns to MONITOR.

3. **MASTER AND VIENO SIGNALS TEST**

The test checks that the two signals are set and reset correctly.

4. **TIMER TEST**

Refer to the TIMER TEST in the TEST DESCRIPTION (section 3.1.1) of the UC3003 program

5. **ACIA TEST**

Refer to the ACIA TEST in the TEST DESCRIPTION (section 3.1.1) of the UC3003 program.

6. INTERRUPT TEST

a) Non-vectored interrupt:

Checks the non-vectored interrupts and associated circuits, in particular tests the input port from which the cause of the interrupt and mask status is read and also the interrupts generated by signals NV1, NV2, NV3 and NV4.

b) Vectored interrupt:

Tests the vectored interrupts and registers for storing the vectors by generating a number of vectors using channel 1 of the timer and the ACIA.

c) Non-maskable software interrupt:

A non-maskable software interrupt is generated and a check made to ensure that the interrupt takes place.

d) Non-maskable interrupt for TCB alarm:

In the test, 15 single errors and a double error are simulated and a check made to see that the interrupt occurs. A check is also made that the NMIBC signal is latched in the correct latch.

e) Non-maskable interrupt (IPC) for implementation of interprocessor communication in multiprocessor environment.
The test provokes an interrupt and checks that it occurs. A further check is made to ensure that the IPC signal is stored correctly in the right latch.

7. ABORT LOGIC TEST

In this test, all the situations resulting in an abort are simulated. Then a check is made that:

- the trap is generated;
- the MMU Status Registers and the hardware register store the correct data.

The memory disable flip-flop is also tested. This test is made by activating both MMU's in order. The segment on which the tests are carried out is <<22>>. Even if there is only one MMU, the test is still performed.

8. **ROM TEST**

The ROM bank is tested by working out the CRC and comparing it with the CRC recorded in the last four bytes of the ROM. The ROM segment can be selected in the MAKEFILE.

9. **EAROM TEST**

Tests carried out:
a) short circuit test;
b) address test;
c) Abraham test.

a) the short circuit test reveals any shorts between bits of a cell.

b) the address test reveals any shorts between locations at different addresses.

c) this is a functional test in which a reduced version of the Abraham-Thatte algorithm is used.

10. **DIP-SWITCHES TEST**

In this test, the status of the board DIP-switches is read. Their status is then compared with the values entered by the operator; where they do not match, the new value read is displayed.

11. **CACHE TESTS**

This test checks the Cache memory available to the CPU in 3 stages:

STEP 1 Tests the memory address TAGs.

STEP 2 Tests the CACHE using a reduced version of the Abraham-Thattle algorithm.

STEP 3 Tests the CACHE WATCH-DOG timer (selected in the preprogram).

Steps 2 and 3 can be carried out in EXTENDED or SHORT version depending on the the selection made in the preprogram.

12. **WATCH-DOG LOGIC TEST**

This test checks that all modifications made to main memory by the CU's are reflected by similar modifications to the Cache memory to ensure that all the CU's at any given time the same information. If there is no Cache, the test is not performed.

13. **BUS ARBITER TEST**

In this test, a program is run in parallel on all the CU's of the system and simultaneous bus accesses attempted to check correct handling of the shared resource. The test is performed with Cache enabled and disabled.

14. RESET TEST

This controlled test performs a Hardware reset of the peripherals connected. The CU is not reset. The system is reset after the test.

3.4.2 ERROR AND SERVICE MESSAGES

Note: If a hardware error is found replace the CU board.

Test 1 messages

- INCORRECT UC MASTER SLOT NUMBER
- MASTER : TEST ERROR
- SLAVE #1/#2 : TEST ERROR

Test 2 messages

- FAULT IN MMU2 STATUS REG. BITS
- URS-BIT FAULT IN MMU2
- FAULT IN MMU1/2 REG.S WR-RD-1/2/3
- FAULT USING MMU1/2 IN RAM ADDRESSING
- FAULT MMU1/2 RAM ADDRESSING FF00 DUAL-PORT RAM

Test 3 messages

- MASTER/VIENO SIGNAL STUCK AT 0/1

Test 4 messages

- COUNTER 0/2 FAULT
- COUNTER 1 INTERRUPT FAULTING
- LATCH OUTPUT CNT1 FAULT

Test 5 messages

- SIGNAL P0x STUCK AT 1/0 OR LATCH FAULT
- SIGNAL P01/P02/P03 OR LATCH FAULT
- TIME-OUT ERROR ON TX/RX READY
- DOUBLE BUFFERING FAULT
- ERROR FLAGS STUCK AT 0/1
- FRAMING/OVERRUN/PARITY ERROR

- WRONG DATA RECEIVED
- TIME-OUT ERROR ON LAST TX DATA
- UNKNOWN INTERRUPT

Test 6 messages

- NVx & ENx: WROTE 1/0 READ 0/1 : verify NVx and ENx signals
- INTERRUPT NV1/NV2/NV3/NV4 FAULT
- NV1/NV2/NV3/NV4 INTERRUPT MASK FAULT
- CONCURRENT INTERRUPT FAULT
- NO TIMER INTERRUPT
- BAD VECTOR TIMER/ACIA INTERRUPT
- NO IPC INTERRUPT
- IPC SIGNAL OR LATCH FAULT
- NMI SOFTWARE NOT OCCURRED
- NO ALARM TCB INTERRUPT (WARMA/NOMIN)
- LATCH NMI FAULT

Test 7 messages

- VIOL.TYPE REG. FLAGS FAULT : Violation Type Register fault
- VIOL.TYPE REG. FAULT : Violation Type Register fault
- VIOL.SEG.NUM.REG. FAULT : Violation Segment Number Register fault
- VIOL. OFF.REG. FAULT : Violation Offset Register fault
- BUS CYCLE STATUS REG. FAULT
- INST.SEG.NUM.REG.FAULT : Instruction Segment Number Register fault
- INST.OFF.REG FAULT : Instruction Offset Register fault
- HW REGISTER FAULT
- RDV/SYSV/EXCV TRAP NOT OCCURRED
- CPUIV/EXCV/PWW TRAP OCCURRED
- FATAL CONDITION FAULT
- FATAL FLAG STUCK AT 0

- ENABLE/DISABLE INHIBITION MEMORY FAULT

Test 8 messages

- LOW/HIGH BANK FAULT

- BANK FAULT

Test 9 messages

- SHORT DATA/ADDRESS ERROR ON EAROM

- EAROM NOT TYPE 64 X 4

Test 10 messages

- SWITCH ON BOARD UC SLOT - X
  READ IN0 = X EXPECTED Y
  READ IN1 = X EXPECTED Y
  READ IN2 = X EXPECTED Y
  READ IN3 = X EXPECTED Y

Test 11 messages

- TAG TEST: FOUND HIT INSTEAD OF MISS

- FOUND HIT/MISS INSTEAD OF MISS/HIT

- DATA COMPARE ERROR

- FOUND MISS INSTEAD OF HIT IN WR-LOOP

- RANDO FLIP FLOP ERROR

- FLEX DISK ERROR

- FLEX DISK RESET ERROR

- HARD DISK INPUT/OUTPUT ERROR

Test 12 messages

- WATCH DOG ERROR

- NO CACHE

Test 13 messages

- MODE PARAMETER ERROR

- TARGET CPU NOT PRESENT/READY

- TARGET NAME SAME AS SOURCE NAME

- TARGET CPU DOES NOT ACKNOWLEDGE

3.6 FJCAC1: CACHE UC070 WITH XU1700/1703 TEST PROGRAM

PROGRAM PURPOSE

This program operates on a subsystem made up of an extra fast 3000SV basic unit composed of a CPU board with cache memory and a FUJITSU hard disk unit.
The program tests the operation of all the parts regarding the cache and checks that the hard disk unit is connected correctly.

HARDWARE REQUIRED

UC070 extra fast CPU board, RAM board, floppy/mini-floppy disk controller, display-keyboard controller, FUJITSU hard disk controller.

WARNING

The cache is disabled at the end of the test.

LOADING PROCEDURES

Refer to section 1.3.2.

3.6.1 TEST DESCRIPTION

The tests for this program are the same as those for the 51CAC1 program (section 3.5.1).

3.6.2 ERROR MESSAGES

The error messages produced by this program are the same as those produced by the 51CAC1 program (section 3.5.2).

3.7 WRCAC2: CACHE UC070 WITH 1707/XU1709 TEST PROGRAM

PROGRAM PURPOSE

This program operates on a subsystem made up of an extra fast 30005V basic unit composed of a CPU board with cache memory and a WREN hard disk unit.
The program tests the operation of all the parts regarding the cache and checks that the hard disk unit is connected correctly.

HARDWARE REQUIRED

UC070 extra fast CPU board, RAM board, floppy/mini-floppy disk controller, display-keyboard controller, WREN hard disk controller.

WARNING

The cache is disabled at the end of the test.

LOADING PROCEDURES

Refer to section 1.3.2.

3.7.1 TEST DESCRIPTION

The tests for this program are the same as for those in the 51CAC1 program (section 3.5.1).

3.7.2 ERROR MESSAGES

The error messages produced by this program are the same as those produced by the 51CAC1 program (section 3.5.2).

3.8 MEM813: RAM TEST PROGRAM

PROGRAM PURPOSE

To check the RAM on M30, M31, M34, M40, M44 systems and/or the ECC on a modified M54/64 system.

HARDWARE REQUIRED

RAM TEST: boards ME019/24/27/32/ or RA057/57/A

ECC TEST: RA065 and UC070 modified to Olivetti Mod. Request 963993K-P;

cable: PIN 13 ON CPU 8 x 2 CONNECTOR TO PIN 17 ON RAM EDGE CONNECTOR
PIN 16 " " " " PIN 21 " " "

GENERAL

There are two levels of test provided in the program:

a) level 1 - SHORT TEST

This test uses the short version of the Abraham-Thatte algorithm to test the RAM and provides minumum test cover.

b) level 2 - LONG TEST

This test uses the long version of the Abraham-Thatte algorithm to test the RAM and provides a maximum test cover.

LOADING PROCEDURES

Refer to section 1.3.2

PRELIMINARY INSTRUCTIONS

SHORT TEST

1. Access MONITOR and Select MONITOR HELP menu

2. Select ANSWER LEVEL command

3. Set ANSWER LEVEL to 0, and then load the program.

LONG TEST (approx. 20 minutes for 128k bytes see test description)

Load program, then select one of the following tests according to requirements:

1. Check on system memory and area containing the monitor.

   Run:

   - TEST 5 of MENU, to display the physical address map for sizes equal to or greater than 128k bytes,

   - TEST 7 of MENU to execute test.

2. Search for faults in system memory.

   Insert an operational memory board sufficient to contain the Monitor and Diagnostic program at low addresses, not contiguous to the zone to be tested and load Monitor and Test program. Run:

   - TEST 5 of MENU, to display the physical address map for sizes equal to or greater than 128k bytes,

   - TEST 3 of MENU, to remove the first block appearing in the physical map,

   - TEST 7 of MENU, to execute test.

3. Test on video controller memory.

   Run:

   - TEST 5 of MENU, to display the physical address map,

   - TEST 6 of MENU, to include in test all memory blocks less than 128k bytes,

   - TEST 3 of MENU, to remove blocks not relevant to the test,

   - TEST 4 of MENU, to correct initialization and end of test address,

   - TEST 7 of MENU, to execute test.

4. Test on ECC memory.

   Connector cable between RAM and CPU as indicated below then run:

   - TEST 5 of MENU, to display the physical address map,

   - TEST 7 of MENU, to select ECC test,

   - TEST 8 of MENU, to execute test.

3.8.1 TEST DESCRIPTION

SHORT CIRCUIT TEST

Used to reveal any shorts between data bits or bits blocked at 1 or 0. The memory is tested at a given address, the address is then incremented and test repeated until the required memory area is scanned. A total of 34 different test patterns are used. The test duration is approximately 1 min. 30 secs. for each 128k bytes of memory tested.

LONG WORD ACCESS TEST

This test permits a read or write cycle, to immediately follow a read cycle. The aim of the test is to access the memory in the shortest time possible. Test duration is in the order of several seconds for each 128k bytes of memory tested.

REFRESH LOGIC TEST

In this test, a background pattern is written throughout the memory, the memory contents are then checked and the bus cycle suspended for 60secs. with the CPU halted. Test duration is a minimum of 120 secs. plus the time required to access the whole of the memory six times.

SHIFTED DIAGONAL TEST

The purpose of this test is to verify that the recovery times of the amplifiers are correct and to operate the decoders under critical conditions. The test is performed on 16 memory chips at a time, the number of rows being defined by the default parameters.

The memory is first written with the background pattern and then, starting from the top left-hand corner, the diagonal is written with the test pattern. The entire memory is read in columns, and tests repeated shifting the diagonal to the right by one column until all rows are covered. The test execution time is approximately 20 minutes for each 128k bytes of memory tested and changes linearly and proportional to the memory size.

ABRAHAM-THATTE FUNCTIONAL TEST

This test is an algorithm, used to detect error conditions, not at gate level, as with the previous tests, but at the level of the functional blocks. Two test versions are provided: a short version and a long version. The short version execution time is several seconds whilst the long version execution time is approximately 20 minutes for each 128k bytes of memory tested.

ECC TEST

This test checks the ECC logic. Writes 16 double words with the ECC enabled. Reads the words written with the ECC disabled. Changes a bit of the data read (hence writes new data with one bit different from previous read) with the ECC disabled. Reads the data with the ECC enabled and hence checks that the bit previously set is corrected. If the error is not corrected a message is given to indicate the error.

ERROR MESSAGES

All the error messages are accompanied by an 8 digit hex. code with the the following format: "0000 XY00".

Where: X = 0, indicates physical address map error
X = 1, indicates out of memory error
X = 2, indicates a read error
X = 4, indicates a parity error.

Y = number of times the error has occured less 1.

Note: Also compound errors are indicated, thus X = 6 indicates read error (2) + parity error (4).

- ***** privileged instruction trap ***** = execution of system instruction in user mode

- ***** segment trap *****

- ***** non maskable interrupt ***** = non-maskable interrupt for out of memory

To regain system control after receiving one of these messages the system must be reset.

- **block XX bad start or end address** = the block start address does not correspond to the first byte of a long word, or the end address does not correspond to the last byte, or the start address is equal to or greater than the end address.

- **block XX block address is ROM address** = at least one address of block XX is in the first physical segment reserved for the ROM.

- **block XX on monitor address space** = at least one address block XX is in the space reserved for the monitor.

- **block XX already in physical map** = block containing Monitor is already listed in physical map.

- ***** short memory length ***** = system memory is less than the required size when a monitor zone test has been requested.

- *** X * at add. 00yyyyyy read wwww (zzzz)** = during execution of test X, the word read at address yyyyyy is wwww instead of zzzz.

- *** X * at add. 00yyyyyy no memory ready** = during execution of test X, at address yyyyyy an out of memory signal has been received.

- *** X * at add. 00yyyyyy parity error** = during execution of test X, at address yyyyyy a parity bit error signal has been received.

SUMMARY MESSAGES

At the end of each memory scan, the program issues a message on the diagnostic line in the following format:

test X * block YY * fault WW * hh : mm : ss

Where:

X = the current test number, with:

1: Short circuit test

2: Long Word Access Test

3: "Shifted" Diagonal Test

4: Refresh Logic Test

5: Abraham-Thatte Functional Test (long/short)

6: ECC test

YY = The memory block being tested

WW = The number of errors found during time h

hh:mm:ss = The test execution time in hours, minutes and seconds.

3.8.2 LOCATION OF FAULTY CHIP

The co-ordinates to locate the position of the faulty chip are obtained from the following tables, as indicated in the example:

```
ERROR MESSAGES: * 1 * at add. 00284760 parity error
                * 1 * at add. 00284760 read 0081 (0001)

GIVEN:          RA57 board (256 Kbits per chip)

THUS:           ERROR = PARITY ERROR
                ERROR ADD = 284760
                WRITE data = 0001;  READ data = 0081
                START ADD. = 200000 (as defined in MENU - TEST no 5)
```

1. Calculate the address OFFSET by subtracting the START ADD from the ERROR ADD (both indicated on the display). i.e. 284760 - 200000 = 084760

2. Determine the ADDRESS RANGE or bank in which the OFFSET value falls. Thus (a) ADDRESS RANGE (for OFFSET 084760) = 080000 - 0FFFFFF (or bank 2).

3. Determine the ADDRESS BIT containing the error by comparing data read with data written.

BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ 0081 (hex) =	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
WRITE 0001 (hex) =	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
DIFFERENCE	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-

Thus (b): incorrect ADDRESS BIT = 7.

4. Using results (a) and (b) and referring to the RA57 (256 Kbits/chip) table, the location of the faulty RAM = Q09-1 (bank2). See PCB layout documentation for the significance of Q09-1 location codes.

NOTES:

If there are an even number of bits in error in the same word or byte, "PARITY ERROR" is NOT indicated.

If the error is on one of the two parity chips and has been detected during test no 1 (SHORT CIRCUIT TEST) an odd address is displayed for the least significant byte (bits 0 to 7), and an even address is displayed for the most significant byte (bits 8 to 15).

If there are more than one RAM board, the board containing the error is determined by the START ADDRESS and the available RAM space on each board.

GIVEN: RA57A board of 2 Mbytes and RA57C board of 1 Mbyte
START ADD = 200000 ERROR ADD = 4E7BC0

1) (a) Calculate OFFSET due to START ADD.
i.e. 4E7BC0 - 200000 = 2E7BC0 (since START ADD = 200000)
(b) Calculate OFFSET due to first board (2 Mbytes board)
i.e. 2E7BC0 - 200000 = 0E7BC0 (since 2 Mbyte = 200000hex)

2) Therefore the second board (1 Mbyte board) contains the error where ADDRESS RANGE (for OFFSET 0E7BC0) = 080000 - 0FFFFF.

ME019 BOARD WITH 16 KBIT CHIPS

ADDRESS BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
000000-007FFF	A05	B05	C05	D05	E05	F05	G05	L05	A06	B06	C06	D06	E06	F06	G06	L06
008000-00FFFF	A07	B07	C07	D07	E07	F07	G07	L07	A08	B08	C08	D08	E08	F08	G08	L08
010000-017FFF	A09	B09	C09	D09	E09	F09	G09	L09	A10	B10	C10	D10	E10	F10	G10	L10
018000-01FFFF	N06	P06	R07	Q07	P07	N07	N07	P07	R08	R09	Q09	P09	N09	N10	P10	Q10

ME024 BOARD WITH 16 KBIT CHIPS

ADDRESS BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
000000-007FFF	L03	G03	F03	E03	D03	C03	B03	A04	L04	G04	F04	E04	D04	C04	B04	A04
008000-00FFFF	L05	G05	F05	E05	D05	C05	B05	A05	L06	G06	F06	E06	D06	C06	B06	A06
010000-017FFF	L07	G07	F07	E07	D07	C07	B07	A07	L08	G08	F08	E08	D08	C08	B08	A08
018000-01FFFF	L09	G09	F09	E09	D09	C09	B09	A09	L10	G10	F10	E10	D10	C10	B10	A10

ME032 AND ME027 BOARDS WITH 64 KBIT CHIPS

ADDRESS BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
000000-01FFFF	A03	B03	C03	D03	E03	F03	G03	L04	A04	B04	C04	D04	E04	F04	G04	L04
020000-03FFFF	A05	B05	C05	D05	E05	F05	G05	L05	A06	B06	C06	D06	E06	F06	G06	L06
040000-05FFFF	A07	B07	C07	D07	E07	F07	G07	L07	A08	B08	C08	D08	E08	F08	G08	L08
060000-07FFFF	A09	B09	C09	D09	E09	F09	G09	L09	A10	B10	C10	D10	E10	F10	G10	L10

RA057 AND RA57 BOARDS WITH 64 KBIT CHIPS

ADDRESS BITS	0	1	2	3	4	5	6	7
000000-01FFFF	E10	F10	G10	L10	M10	N10	P10	Q10
020000-03FFFF	E09-1	F09-1	G09-1	L09-1	M09-1	N09-1	P09-1	Q09-1
040000-05FFFF	E08-3	F08-3	G08-3	L08-3	M08-3	N08-3	P08-3	Q08-3
060000-07FFFF	E07-5	F07-5	G07-5	L07-5	M07-5	N07-5	P07-5	Q07-5

ADDRESS BITS	8	9	10	11	12	13	14	15
000000-01FFFF	E06-7	F06-7	G06-7	L06-7	M06-7	N06-7	P06-7	Q06-7
020000-03FFFF	E05-9	F05-9	G05-9	L05-9	M05-9	N05-9	P05-9	Q05-9
040000-05FFFF	E05-N	F05-N	G05-N	L05-N	M05-N	N05-N	P05-N	Q05-N
060000-07FFFF	E04-L	F04-L	G04-L	L04-L	M04-L	N04-L	P04-L	Q04-L

RA057 AND RA57 WITH 256K BIT CHIPS

ADDRESS BITS	0	1	2	3	4	5	6	7
000000-07FFFF	E10	F10	G10	L10	M10	N10	P10	Q10
080000-0FFFFF	E09-1	F09-1	G09-1	L09-1	M09-1	N09-1	P09-1	Q09-1
100000-17FFFF	E08-3	F08-3	G08-3	L08-3	M08-3	N08-3	P08-3	Q08-3
180000-1FFFFF	E07-5	F07-5	G07-5	L07-5	M07-5	N07-5	P07-5	Q07-5

ADDRESS BITS	8	9	10	11	12	13	14	15
000000-07FFFF	E06-7	F06-7	G06-7	L06-7	M06-7	N06-7	P06-7	Q06-7
080000-0FFFFF	E05-9	F05-9	G05-9	L05-9	M05-9	N05-9	P05-9	Q05-9
100000-17FFFF	E05-N	F05-N	G05-N	L05-N	M05-N	N05-N	P05-N	Q05-N
180000-1FFFFF	E04-L	F04-L	G04-L	L04-L	M04-L	N04-L	P04-L	Q04-L

3.9 EARUT3: INSTALLATION OF LINE PARAMETERS ON EAROM PROGRAM

PROGRAM PURPOSE

To enable EAROMs to be initialized with correct line parameters and to read and modify these parameters to suit the system hardware.

HARDWARE REQUIRED

UC042 CPU board, RAM board, line controller(s).

GENERAL

The program caters for STANDARD MOS, OSLEM and CONFINFO systems.

LOADING PROCEDURE

Refer to section 1.3.2

3.9.1 PROGRAM DESCRIPTION

The parameters are installed in 4 fields between addresses E004 and E04F. The first three fields are dedicated to STANDARD MOS or OSLEM systems whilst the fourth field is dedicated to the STANDARD MOS, OSLEM or CONFINFO system. Each field or block is used for one system only. For security reasons data in the UNBUNDLING field is not accessible.

NOTE

When selecting required field or block 5 is used to select the CONFINO field. The CONFINO field is used only in cluster configurations.

3.9.2 ERROR MESSAGES

There are no error messages specific to this program.

3.10 CHY100: CENTRAL UNIT BOARD UC071 TEST PROGRAM

PROGRAM PURPOSE

To test the MMU and CACHE on the UC071 CPU when connected to various L1 HDU and FDU systems.

HARDWARE REQUIRED

UC071 board and any L1 HDU/FDU system.

LOADING PROCEDURES

Refer to section 1.3.2.

3.10.1 TEST DESCRIPTION

Initially a test is made to ensures that the TCB is in the correct slot as entered by the operator and then the MMU and CACHE tests are executed.

Refer to the corresponding test headings in section 3.4.1 of the UCY805 program for test description.

3.10.2 ERROR MESSAGES

Refer to the corresponding test headings in section 3.4.2.

3.11 TCM802: TCM BOARD TEST

PROGRAM PURPOSE

To check that the TCM board functions correctly.

HARDWARE REQUIRED

TCM board.

LOADING PROCEDURES

Refer to section 1.3.2.

3.11.1 TEST DESCRIPTION

1) ORDER & STATUS REGISTERS TEST

The status register is read and signal DECC0 is tested. When at logic level "0", this signal enables the ECC; if it is at "1", a blocking error occurs and the program is interrupted.

The status register is read and tested to see that it has been cleared. If any of the bits is "1", a blocking error occurs and the program is interrupted.

N.B. if the program is launched in a loop, only the first step of the test (i.e. after a reset) is significant.

The order register bits are set one at a time and the status register is read to check that they are set and then reset.

2) ERROR LOGGING MEMORY TEST

A double word is written with all bits at "0" (with ECC enabled) and then a double word with all bits shifted to "1" (with ECC disabled and error logging enabled) is written.

The first double word written is read and any interrupt is signalled.

Error logging is disabled, the nomin is enabled, and the double word is read back.

Error logging is then reenabled, the double word is read again and an error is indicated if no non-maskable interrupt (NMI) is generated.

The test then verifies that the syndrome for the data written in RAM is correct and the memory area used in the test is reset.

3) ECC TEST

The test checks that there are no short circuits between the status register bits which are to contain the control code or the syndrome pattern.

The test checks that the ECC calculates the control pattern correctly during writes, that the control pattern read in memory is stored in the status register during reads, and that signals SERR0 and MERR0 remain at "0".

32 single errors are generated and the test checks that the ECC calculates the syndrome pattern correctly.

The test then checks that the ECC sends the correct data on the bus when a single error occurs.

4) MULTIPLE ERROR TEST

Double errors are caused on some data written in memory. The data is read and the test checks that signal MERR0 goes to "1".

At the end of the test, the area of memory which has been altered is restored.

5) SINGLE ERROR TEST

Errors on a single bit are generated on some data written in memory. The data is read and the test checks that signal SERR0 goes to "1" and that signal MERR0 goes to "0".

At the end of the test, the area of memory which has been altered is restored.

6) NOMIN TEST

The ECC is disabled and data equal to 3 (2 bad bits) is written to memory. The data is read and the test checks that no NMI has been generated and that the NOMIN bit is at "0".

The nomin is enabled, the data is read back and the test checks that the NOMIN bit is at "1".

7) ARRAY REFRESH TEST

Any soft errors are cleared with an array refresh.

8) BURST TEST

The "BURST" protocol is started by addressing the first double word. The test checks that the 3 subsequent double words are correctly addressed (by revolving address bits ADA20 and ADA30).

N.B. This test is only run if the CACHE ENABLE option has been selected.

4.1 PRGEN3: PRINTERS TEST

PROGRAM PURPOSE

To check the correct operation of the printer connected to the ELB 3684 or the D-BOX (via MUX), to the TWIN controller, to the serial output of the CU board, the CONSOLE or the ELB 1382.

This test program should be used in place of the following programs: PRT.UC, PRTWIN, PRTELB and PRMUX0.

HARDWARE REQUIRED

ELB 3683 (BA126/G0239), or D-BOX and external hardware loopback connector and board MUX G0322; board TWIN G0151 or G0327 (fast); or ELB 1382 (G0189/G0269).

LOOPBACK CONNECTOR

When connected via D-BOX, an external hardware loopback connector must be used; this is connected to the C.L. or RS232 line connector of the D-BOX dedicated to the printer.
The loopback connector is formed by connecting the following pins:

2 <---> 3 4 <---> 5 <---> 8 6 <---> 20

PRELIMINARY OPERATIONS

Before entering the preprogram parameters check that printer parameters correspond with the DIP-switch settings.

Activate the printer, print the diagnostic strip (if available on model) and make sure the printer is not in local mode.

CAUTION

The program operates with printers jumpered for digital break XON-XOFF (DC1/DC3) and does not handle analogue breaks.

When connected with ELB 1382, the program must be launched from the system work station and not from the WS connected to the ELB 1382.

N.B. The time-out, for all input/output operations, has been set for 30 seconds.

LOADING PROCEDURES

Refer to section 1.3.2.

4.1.1 TEST DESCRIPTION

GENERAL

The tests listed in the menu can be re-cycled or skipped with the exception of test 1 which cannot be skipped.

INITIALIZATION

The test checks that the slot selected by the operator contains the controller board.

When connection is via MUX, the MUX should be reset.

Before test execution, the lines and channels are initilaized with the parameters entered by the operator.

1) SELF DIAGNOSTIC WS TEST

This test is run on systems connected with the ELB 3683 (via MUX).

The WS configuration is checked and displayed on the WS monitor. The line number (values from 1 to 4), the ROM type, the RS232 channel used (A or B) and whether the keyboard is connected are indicated.

The line selected is programmed with the WS SET-UP parameters. The service channel and the video/keyboard are initialised. The WS autodiagnostic state is read.

N.B. In order to have the updated status, the WS should be switched off and then on again before launching the test.

1) ON LINE LOOPBACK TEST

This test is run on systems connected to the D-BOX (via MUX).

The test is only run if a loopback connector is installed on the C.L. or the D-BOX RS232 line dedicated to the printer under test. The MUX line under test is programmed as follows:

```
     SPEED = 19200 BPS
    PARITY = NO
  STOP BIT = 1
BIT LENGTH = 8
```

The test consists of transmitting data from a buffer, and at the end of transmission comparing the data in the receive buffer with the transmitted data.

N.B. This test requires loopback connectors also the cycle number must be selected as it is not selected by default.

1) CONNECTION PRINTER TEST

This test is carried out when connection is made via CU, CONSOLE, TWIN or via ELB 1382. The test checks the printer connection.

2) SET GRAPHIC PRINTER TEST

The printer graphics set (ISO characters) is printed out. The disalignment of the left margin should be less than 0.4 mm.

3) QUALITY PRINTER TEST

A number of rows containing ISO characters is printed out. The characters are shifted by one character position for each row. The number of rows printed is equal to the number of characters per row.

4) HORIZONTAL ALIGNMENT PRINTER TEST

A row of "_" characters is printed.

5) VERTICAL ALIGNMENT PRINTER TEST

A row of "E" characters is printed.

6) HORIZONTAL SPACE PRINTER TEST

A row of "H" characters is printed with spacing between characters.

7) LINE FEED PRINTER TEST

A row of "E" characters with line feed is printed followed by another row of "E" characters.

The line feed pitch should be equal to 5.08 +/- 0.005 mm for printers with 1/5" pitch, and equal to 4.23 +/- 0.005 mm for printers with 1/6" pitch.

8) HEAD MOVEMENT PRINTER TEST

Four rows of "E" characters with line feed are printed. The first and third rows is printed from left to right and then the second and fourth rows from right to left.

9) OPTIMIZATION PRINTER TEST

A series of rows of "H" characters is printed, each row being two characters shorter than the previous row (one character less at each margin). The head should optimize its course and not return to the left margin each time a row is printed.

4.1.2 ERROR AND SERVICE MESSAGES

ERROR MESSAGES

The error messages are displayed on the WS monitor and can be divided into the following groups:

Blocking Errors

- ***** PRIVILEGED INSTRUCTION TRAP *****
- ***** SEGMENT TRAP *****
- ***** NON MASKABLE INTERRUPT *****

If blocking errors occur, the system should be reset.

System Errors

- **THE PRESENT CONTROLLER IN SLOT XX ANSWERS PHYSICAL NAME YY INSTEAD OF** ZZ
- **THE SLOT XX IS EITHER EMPTY OR CONTAINS A NOT SELFDECLARING** CONTROLLER
- **UNAVAILABLE PRINTER ERROR** = Error because the printer is not on line, or is switched off. When connection is effected with ELB 1382, the WS may be switched off in which case the ELB should be reset (by switching it off then on again).
- **PRINTER OFF** = The printer is switched off, not connected or incorrect parameters entered.
- **LINE ERROR** Check line connection on the service channel, WS keyboard/video channel and between WS and DEMULTIPLEXOR.
- **LOCAL UP** Check "local" switch, paper, ribbon etc.
- **SUB RANGE LENGTH ERROR** Indicates that the operator has selected a row length equal to 1 or 2 characters for test 9. This test can only be executed with longer rows.
- **INCOHERENT ERROR MESSAGE REPEAT TEST** = Unknown error try repeating test.

MUX/DEMUX/ELB(3683) - Printer Errors

- **BUFFER RX EMPTY/NOT EMPTY ERROR** = Hardware error caused by the MUX or the PR.
- **REMOTE LOOP BACK ERROR** Check jumpers on the D-BOX (see description of test 1 executed in transparent mode).
- **COMPARE DATA ERROR** = Data from the transmit buffer does not agree with data in the receive buffer; check connection between MUX, D-BOX

and T-BOX.

- **END COMMAND ERROR** = Error while waiting for the end of command interrupt.

- **CHANNEL INITIALIZATION ERROR**

- **CHANNEL ON READ ERROR** = Line error verified while data was being received from the printer.

- **CHANNEL ON WRITE ERROR** = Error due to WS swithed off or in local mode or if length of characters string transmitted is too long.

- **BUFFER RX OVERFLOW ERROR** Check MUX.

- **NO CONNECTION D_BOX - PRINTER** Check connection between the RS232 printer cable and the D-BOX.

- **CONTROL CHANNEL INIT. ERROR** = The WS service channel has not been initialized due to MUX/WS hardware errors or because incorrect line configuration parameters have been entered.

- **KEYBOARD/VIDEO CHANNEL INIT. ERROR** = The WS keyboard/video channel has not been initialized; Check MUX.

- **NO CONNECTION W.S. - PRINTER** Cable between WS and printer is not connected.

- **UNAVAILABLE W.S. ERROR** = The WS is not available because it is switched off or not connected.

- **CONTROL CHANNEL RD/WR ERROR** = Error during the WS autodiagnostic read phase (test 1); verify the WS hardware and connection between WS and DEMULTIPLEXOR.

- **HARDWARE W.S. ERROR** = Hardware blocking error on the WS; the red LED on the front panel of the printer remains on.

- **VIDEO NOT PRESENT ERROR** = The video is not connected to the WS.

- **VIDEO TEST ERROR** = WS video hardware error condition.

- **SELF KEYBOARD TEST ERROR** = WS keyboard hardware error condition.

- **SIO1/2 CHANNEL A/B ERROR** = SIO 1/2 (RS232 channel A/B) hardware error condition.

- **CTC1 CHANNEL 0/1/2/3 ERROR** = Error on transmission channel indicated.

- **NO EXIT NMI DURING RESET PHASE** = The reset was not performed.

- **ERROR** = message displayed on the WS video if there is an error during execution of tests 2 to 9 (relative to MUX/WS/PRINTER connection).

- **LINE CONFIGURATION ERROR** = Hardware error caused by the MUX during line configuration.

CU/Console - Printer errors

- **NO CONNECTION UC - PRINTER** = The printer and the CU are not connected.

- **INCOHERENT CONFIGURATION - ERROR** = Line parameters entered are incompatible with those required.

ELB 1382 - Printer errors

- **LINE ERROR FROM ELB** = ELB connection error.

- **UNAVAILABLE ELB - NO CONNECTION** = The printer and the ELB are not connected, the ELB is switched off or has been switched off during test execution.

- **BUFFER OVERFLOW ON ELB** = Input/output buffer overflow on ELB has occurred; reduce the transmission speed between system - ELB.

- **ELB RESET ERROR**

- **ELB AUTODIAGNOSTIC ERROR** = An error has occurred during the ELB autodiagnostics; verify the hardware and replace the ELB if necessary.

TWIN - Printer errors

- **NO CONNECTION TWIN - PRINTER** = The printer and the TWIN board are not connected.

SERVICE MESSAGES

- **SOFTWARE/HARDWARE RELEASE WS: X.Y**

- **WS TYPE IDENTIFICATION NUMBER: ELB 3683/3684/INCOHERENT (unknown)**

- **CHARACTER GENERATOR ROM TYPE: PK3Z/Y/INCOHERENT(unknown)**

- **KEYBOARD PRESENT/NOT PRESENT**

- **RS232_C LINE A/B CONNECTED/NOT CONNECTED**

4.2 PRTWIN: PRINTER TEST PROGRAM - VIA TWIN CONTROLLER

This program has been replaced by the PRGEN1 program described in section 4.1.

4.3 PRTELB: PRINTER TEST PROGRAM – VIA ELB ADAPTOR

This program has been replaced by the PRGEN1 program described in section 4.1.

4.2 PINBDG: PIN-PAD/BADGE READER TEST PROGRAM

PROGRAM PURPOSE

To verify proper operation of PIN-Pad/Badge Reader controller and peripherals connected to it.

HARDWARE REQUIRED

PIN-Pad/Badge Reader controller (G0195) and PIN-Pad (PIN1440) or Badge Reader XU 1003/1020.

NOTE

1. Test 1 requires a loop plug on the controller I/O connector as indicated:

Pin C linked to Pin 3,	Pin K linked to Pin 10,
Pin E linked to Pin 4,	Pin J linked to Pin L,
Pin H linked to Pin B,	Pin R linked to Pin M,

2. Tests 3 and 4 require a badge with STANDARD RECORDINGS on track 2.

3. Tests 6 and 7 require a sample badge.

4. Test 5 requires a Scratch badge for writing.

LOADING PROCEDURES

Refer to section 1.3.2

4.2.1 TEST DESCRIPTION

The DEFAULT TEST is carried out each time the program starts. This test checks the status of the following signals:

a) during reset:

- INXA0, INXB0
- LOPA0, LOPB0
- TXDA0, TXDB0
- RTSA0, RTSB0
- MODB0

b) after reset:

- TK3A0, TK3B0
- MODB0.

At the start of each test listed in the MENU a CONGRUENCY TEST is carried out in order to make sure that the BADGE READER/PIN PAD (or loop plug in the case of test 1) is connected to the selected controller channel.

The function of each of the tests available is described below:

1. Channel A and then Channel B are tested using the loop plug in the following way:

   tests the "Clear to Send" circuit (CTS), transmits in asynchronous mode a string of 107 consecutive hex. characters via the loop plug and then compares the data transmitted with the data received.

2. Tests the operation of the keys on the PIN-Pad by indicating the key operated on the display and in particular checks that simultaneous operation of keys does not cause an error.

3. Reads track 2 of the sample badge using the XU1003 badge reader and compares the data read with the data written in the program; then checks that the badge-in badge-out interrupt generated by inserting and removing the badge is correctly synchronized with the program.

4. Tests the XU1020 badge reader as in test 3 but omitting the interrupt tests.

5. Writes a sequence of 107 consecutive hex. characters, on the 3rd track of the scratch badge, then reads the badge and compares the data read with the data written; in addition the program checks the generation of the badge-in/badge-out interrupts as in test 3.

6. Reads the string written on the 2nd track of the sample XU1006 badge, tests the STX (0B) and ETX (1F) control characters, carries out the vertical and longitudinal redundacy checks, checks the badge-in/badge-out interrupts, and finally compares the data read with another read of the same track.

7. Tests the XU1020 badge reader as in test 6 but omitting the interrupt tests.

4.2.2 REPLIES TO ERRORS

The error messages are self-explanatory when taken into consideration the context of the tests.

There are also some specific messages:

```
**LOGIC NAME NOT FOUND IN DDB-TAB**
! UNRECOVERABLE ERROR !
RESET and LOAD PROG.
```

This indicates that the slot number entered in the pre-program is incorrect or that it does NOT contain the PIN-Pad/Badge reader controller.

The error can only be recovered by resetting the system, reloading the program and entering the correct CONTROLLER NUMBER in the pre-program.

```
* CONGRUENCE TEST*
XXXXX CONNECTION MISSING (XXXXX = peripheral name)
! UNRECOVERABLE ERROR !
RESET and LOAD PROG.
```

This indicates that the cable connection to the peripheral is missing.

```
CMD: command name MVO
   * REJECTED *
```

Indicates that the MVO Command has been rejected.

```
   *DEFAULT TEST *
UNFORESEEN STATUS ON SIGNAL
   YYYYYY (YYYYYY = signal name)
```

This indicates the signal has caused a status error during the DEFAULT TEST.

```
* TIME-OUT ON TRANSMISSION *
! UNRECOVERABLE ERROR !
RESET and LOOP PROG.
```

This indicates controller and peripheral transmission errors and suggests that test 1 (LOOP PLUG TEST) be carried out.

4.3 PINELB : PINPAD/BADGE READER (CONNECTED VIA ELB) TEST PROGRAM

PROGRAM PURPOSE

To ensure that PIN-Pad and Badge reader function correctly when connected to the ELB ADAPTOR.

HARDWARE REQUIRED

1381/1382 ELB ADAPTOR, PIN-Pad (PIN1440) and Badge Reader XU 1003.

LOADING PROCEDURES

Refer to section 1.3.2

4.3.1 TEST DESCRIPTION

The function of each test is described below:

1. Determines the status of the adapter and keyboard using diagnostic tests and displays the result on the video.

2. Sets LED on keys to operate in blinking mode and displays the location codes of the keys operated so that the operator can determine if the correct key has been depressed.

3. Reads the badge introduced in the badge reader and displays the data read indicating the last separator with "?" or if characters are considered incorrect with "*".

4. Examines the simultaneous operation of keyboard, PIN-Pad and badge reader and displays the characters read on the video (keyboard characters in hex).

4.4 CA2TS1: CA2000 (VIA TWIN RS 232 CONTROLLER) TEST PROGRAM

PROGRAM PURPOSE

To check that peripherals connected serially to the system on the TWIN controller RS 232 line function correctly.

HARDWARE REQUIRED

TWIN RS 232 controller, CA2000 unit

LOADING PROCEDURES

Refer to section 1.3.2

4.4.1 TEST DESCRIPTION

The program checks that the slot number entered by the operator contains the correct controller; the controller is then initialized and the interface to the CA2000 unit checked; the program then performs the following tests in the order given:

INCOMING DATA TEST*

Checks the CA2000 timer by transmitting a test data string and verifying that the CA2000 responds correctly following an interrupt.

DELAY DURING ANSWER TEST*

Checks that the CA2000 response can be interrupted for varying time periods.

DELAY AFTER TRANSMISSION TEST*

Checks that the CA2000 can delay its response.

TRANSMISSION ERROR TEST*

Checks that the CA2000 can recognise errors in data transmission: four consecutive reset commands are sent out each in a different mode.

EMPTY CASSETTE AND RUN UP/DOWN TEST*

Checks the up and down movement of the hoppers (hoppers must be empty).

REQUEST FORMAT ERROR TEST*

Incorrect commands (non-existent or incomplete) are sent to the CA2000 with the hopper lifts in the up position. The CA2000 should respond "request format error". A correct but incomplete command is then sent to the CA2000 - the response should be the same. The hopper lifts are then lowered and correct commands sent out - the CA response should be "lifts down".

* Note: test is not performed if program is run in shared mode.

ILLEGAL CMD OR CMD SEQUENCE TEST*

Checks the CA2000 controls on the format of messages received, in particular on the order of commands and the number of notes.

SINGLE CASSETTE (REJECT) TEST

Checks the move forward and reject commands. There should be no errors in withdrawal of notes from the hoppers.

SINGLE CASSETTE (DELIVERY) TEST

Checks the move forward and delivery commands for each hopper. There should be no errors in withdrawal of notes from the hoppers. One hopper is tested at a time.

MULTIPLE CASSETTES (REJECT) TEST

Checks that the move foward and reject commands are functioning for all hoppers (test continues until one hopper at least is emptied).

MULTIPLE CASSETTES (DELIVERY) TEST

Checks that the move notes forward and delivery commands are functioning correctly on all hoppers (at least one should be emptied).

DISPENSE TEST

The dispense command is sent to the CA2000 to check that it is in good working order. Its responses are checked until one hopper is emptied.

TWO TELLER TEST*

Performed only if test set for two tellers. Notes are dispensed on one teller, then on the other; if the notes are not taken up from the first teller, after a certain period, there should be an error message to indicate incorrect operation of one or both tellers.

* Note: test not performed if program is run in shared mode.

4.4.2 ERROR MESSAGES

- CPU INTERRUPT NETWORK FAULT = no interrupts acknowledged
- CPU ANOMALOUS INTERRUPT = an interrupt foreign to the DART network and not related to the current program has been found
- FRAMING ERROR ON RECEIVING = error in the coding of the message received from the CA2000, error of the CA2000 electronics or the line or the parameters introduced
- OVERRUN ERROR ON RECEIVING = data received overrun before they can be analysed. Check the baud rate.

- PARITY ERROR ON RECEIVING
- UNKNOWN ERROR ON RECEIVING = message received but not recognised
- ERROR ON LRC CHECK
- ERROR ON END OF MSG CHECK
- ERROR ON LRC AND EOM CHECK
- UNEXPECTED INTERRUPT TYPE ON RX
- CA 2000 GENERAL STATUS OK
- CA 2000 STATUS OK ON FORCED ERROR
- LOW LEVEL IN CASSETTE
- REJECTED NOTES ON LAST TRANSITION = check that no notes were dispensed in the last transaction
- REJECT CASSETTE SOON FULL = reject hopper should be emptied
- HIGH PRESSURE IN CASSETTE = hoppers too full
- ERROR ON CA2000 RECEIVING PART
- LIFTS IN CASSETTES ARE DOWN
- CASSETTE NOT FOUND FROM CA 2000
- NOTES TOO LONG IN DELIVERY MODULE = the CA 2000 is not dispensing the notes
- REJECT CASSETTE NOT FOUND FROM CA = CA does not recognise reject hopper
- CA CHECK : NOTES IN DELIVERY THROAT = the notes are still in the dispenser
- DELIVERY THROAT EMPTY, VERIFY = dispenser is empty
- REMOVE NOTES FROM REJECT CASSETTE
- FAILURE TO FEED DISPENSE NOT DONE = check the CA 2000
- NOTES UNDER SENSOR AT START = a CA 2000 mechanical fault
- CLEANING FINGERS NOT IN HOME POSITION
- COUNT SENSOR NOT ACTIVATED FEED = the banknote counter is not on
- WRONG COUNT DETECTED FROM CA 2000
- ERROR IN STACKER DELIVERY = dispenser module not in correct position

- DELIVERY UNIT BUSY AFTER REJECT = after a reject, the dispenser module retains busy status

- TOO MANY NOTES ON CONVEYOR

- MAIN MOTOR ERROR

- GAIN ON LIMIT = motor error: suspend all operations or machine may suffer permanent damage

- UNEXPECTED CA LOCKOUT CONDITION = command received has not been correctly executed

- ABNORMAL CA MESSAGE RECEIVED = command received not recognised by CA 2000

- CASSETTE $$: WRONG IDENTIFIERS = a hopper not identified

- ERROR ON MODULE $$ = hopper error (in the travel or pick up mechanism)

- ERROR ON ALL MODULES DISACTIVATED

- NOTES MORE THAN REQUESTED FEED $$

- NOTES LESS THAN REQUESTED FEED $$

- REJECT TRACE ERROR = service message sent to CA 2000 revealing how many REJECTs have occurred in the last fifteen operations

- TEST SKIPPED

- CONTROL THAT LIFTS NOT DOWN = check the lifts are not down

- WHEN LIFTS DOWN FILL ALL CASSETTES

- REMOVE NOTES FROM DELIVERY IN 5 MIN. = all notes to be removed within five minutes

- TEST NOT EXECUTED, ONLY ONE TELLER

- CA 2000 POWER OFF OR MODM FAULT = for the host, CA2000 is off: check the electronics and that the "on" carrier wave is present

- CA 2000 POWER OFF OR MODM FAULT

4.5 FEEDER: MAGNETIC FEEDER TEST PROGRAM

PROGRAM PURPOSE

To ensure that the front-connected magnetic feeder on printers connected by CPU serial interface is functioning correctly.

HARDWARE REQUIRED

Video controller, 9" or 15" video, keyboard, printer PR 2840, FD or MFDU controller, FDU or MFDU, standard 13 cables (code no. 335681 U: other non-standard cables may, however, be used).

PRELIMINARY OPERATIONS

Power-up the printer and operate the test switch. Verify that the printout is correct then set printer ON LINE.

LOADING PROCEDURES

Refer to section 1.3.2

4.5.1 TESTS DESCRIPTION

TEST 1

Displays the settings specified by the operator in the preprogram; checks that printer is connected and displays magnetic feeder settings.

The test is obligatory when the MONITOR HELP is accessed.

TEST 2

Prints character already set or introduced through the keyboard.

If SAVING BOOK is used, a single line is printed; if a CARD is used, the single line print can be used or a sequence of line prints used where the first and last lines are printed and then the remaining lines starting from the 2nd line and continuing until the card is nearly full.

TEST 3

A recording and reading test is performed on the magnetic strip.

Note: As there is no check on the maximum number of characters to be recorded, an L.R.C. error is signalled if the strip capacity is exceeded.

4.5.2 ERROR AND SERVICE MESSAGES

The error and service messages are listed below:

TYPE OF ERROR	MODE OF EXCHANGE	CAUSES	CHAR. MISS.	ACTION
FEEDER OUT	Controlled mode (status	Feeder missing or jumpers not connected. Program returns to monitor	/	Connect feeder jumpers or change printer
MAGNETIC FEEDER OFF	Controlled mode (status request)	Magnetic feeder missing or jumpers not connected	/	Connect magnetic feeder jumpers
L.R.C. ERROR	Controlled mode (status request)	Recording or reading error on saving book magnetic strip. Program makes five attempts to recover; then proceeds to test end.	/	Change saving book or decrease number of characters to be recorded; if no change magnetic feeder is not working
EMPTY STRIP	Controlled mode (status request)	Message: the saving book magnetic strip is empty - in read only	/	/
INCORRECT RECORDING OR READING	Controlled mode (status request)	Message: (displayed after five errors) L.R.C. ERROR in recording or in reading -program proceeds to 03 test end	/	See L.R.C. ERROR above
INTERRUPT PRINTER OFF	Controlled mode (status request)	Printer switched off during reception of message Program returns to pre-program	/	Turn on printer and clear LOCAL status before restarting program
ALMOST END OF CARD	Controlled mode (status request)	Message: in test 02 sequential printing on CARD when end of form is reached	no	/

TYPE OF ERROR	MODE OF EXCHANGE	CAUSES	CHAR. MISS.	ACTION
TOTAL DIPPING OF CARD	Controlled mode (status request)	Due to total insertion of card. Program returns to MONITOR	yes	/
BURRAGE	Controlled mode (start request)	Due to an impediment in passing document through feeder	yes	Try inserting another document or investigate feeder passage
MISSING CARD OR FEEDER FAULT	Controlled mode (status request)	Due to feeder missing/faulty or card accepted by feeeder being removed during tests		Repair feeder or repeat test
COMMAND ERROR ON ROLLER	Controlled mode (status request)	Issue of command to printer incorrect. Program resets malfunction status	no	Probable roller selection error restart program with correct parameters
COMMAND ERROR ON FEEDER	Controlled mode (status request)	Command to printer issue incorrect. Program resets malfunction status.	no	Feeder command error probably: restart program. Try new printer
PRINTER OFF	Freerunning (Break) Freerunning (xon/xoff)	The printer is switched off at the start program or during program execution	/	Ensure printer is powered up and ON LINE
	Controlled mode (Status)	The program returns to the pre-program		
DIS-CONNECTED I/O PRINTER CABLE	All data exchange modes	RS 232 cable of the printer not connected to S 3000	no	Connect RS 232 cable to S 3000
BUSY BUFFER		Line buffer is full temporarily	no	
BUSY LOCAL FOR:	Freerunning (xon/xoff)	printer is set to LOCAL	no	
OPEN CARTER		Open Carter	no	Lower carter, set printer ON LINE

TYPE OF ERROR	MODE OF EXCHANGE	CAUSES	CHAR. MISS.	ACTION
END OF RIBBON	Freerunning (Break except for PR2400)	End of ribbon	no	Fit new ribbon then set printer ON LINE
END OF PAPER		End of paper	no	Insert paper, perform 3 line feeds, then set printer ON LINE
END BUSY	Freerunning (xon/xoff) Freerunning (break)	Full buffer, local status, open carter, end of ribbon/paper	/	/
LOCAL	Controlled mode (status	Local status * Open cater *	no	Set printer ON LINE and set printer ON LINE
END OF PAPER	Controlled mode (status request)	Paper out	no	Insert paper perform 3 line feeds, set printer ON LINE
OPEN CARTER OR END OF RIBBON	Controlled mode (status request)	Open carter or end of ribbon	/	Close carter, set printer ON LINE
PARITY ERROR	All data exchange modes	Parity error during reception/ transmission	yes	Check printer operating links correspond with entered in the parameters pre-program
OVERRUN ERROR	All data exchange modes	Missing characters	yes	Restart the program, if the error persists change controller/CPU
FRAME ERROR		Synchronization error or wrong transmission or break condition		
CONTROLLER RS 232 FAULT	All data exchange modes	Controller not working	no	Change controller/CPU

TYPE OF ERROR	MODE OF EXCHANGE	CAUSES	CHAR. MISS.	ACTION
BUSY CHANNEL		Busy channel	no	/
IOCB ERROR		Wrong command IOCB MVO	no	Change controller/CPU
COMMAND ERROR		Wrong command to printer.	no	Probable error due to the roller selection; restart the program with the correct parameters.
LINE ERROR	Controlled mode (Status request)	Probable printer error	yes	Try new printer if error persists change controller/CPU
TESTING IN PROGRESS		Continuation of program (e.g. after a blocking error)	/	/
CARD ON THE AUTOMATIC FRONT FEED		Card or passbook present in the automatic front feed operating with roller	/	Remove the card or passbook and continue
PRINTING HEAD OFF	Controlled mode (Status request)	Printing head incorrectly set; the error is signalled by the INT-REQ LED	/	Try switching the printer off and then on again and restarting program (with printer ON LINE)
TIME OUT		Incorrect printer reply to status request		Clear local condition and retry program

Note:

- (*) Not signalled on PR430, at the beginning of the program, when the printer is in local status; not signalled on PR2840 during the program execution when the line is empty.
- (**) Not signalled on PR2840 during the program execution when the line buffer is empty.
- Incorrect characters are often printed due to discrepancies between values entered in the pre-program and settings on the printer.

4.6 SOVRA7: VIDEO/KEYBOARD OVERLAP PROGRAM

PROGRAM PURPOSE

To ensure that the overlap and hardware interrupt mechanisms of the system I/O channels are functioning correctly.

HARDWARE REQUIRED

Floppy disk and minifloppy disk controller, video-keyboard controller, video, keyboard, FDU, MFDU, printer, SMD or integrated HDU controller, XU5010.

PRELIMINARY REQUIREMENTS

For complete overlap of all modules, at least 1 floppy and 1 minifloppy, already formatted, should be available. The system should be initialized in the pre-program phase, after the information contained in track 0 has been read.

The printer, connected to an RS 232 controller, should respond to the XON/OFF operating characteristics with a velocity of 300 baud. The velocity, however, may be altered by the MONITOR HELP program using the hard copy mode. The program automatically interprets and adjusts to the type of video connected.

LOADING PROCEDURES

Refer to section 1.3.2

4.6.1 TEST DESCRIPTION

The program comprises a single test in which the selected controllers are operated in overlap mode using a series of exchange data commands.

Tests carried out on the various units operating in overlapped mode are described below.

FDU

Read, write and data comparison operations are performed in cascade mode using a test pattern. The length of the sequence transmitted is; one sector for disks formatted with 256 bytes/sector and two sectors for disks with 128 bytes/sectors. The test pattern used, comprises characters from 00 to FF which are transmitted in rotation. The operations are repeated for each disk selected.

MFDU

As for the FDU.

HDU (via SMD or XU5010 INTEGRATED controller)

As with the FDU, a series of read, write and check tests is run on the HDU, with the difference, that the transfer length is 1 sector or 64

sectors randomly selected.

The starting sector is also randomly selected.

VIDEO

A series of ISO codes which contain all the commands for the visual attributes are transmitted in rotation to the video. When the type of video has been ascertained, a sequence of characters sufficent to occupy approx. 1/4 of the available video space is displayed. The remaing video space is used for displaying the diagnostic messages.

KEYBOARD

The keyboard is made available to the operator for inputting a series of overlapping characters which are sent to the video and displayed on the status line. Confirmation of input is given by the flashing letter I (input) in a square; to remove, type ENTER.

PRINTER

A series of ISO characters, starting from 1, and increasing to 80 are transmitted to the printer in incremental steps of 1 character. The sequence is then repeated.

4.6.2 ERROR AND SERVICE MESSAGES

A list of messages is given below together with notes:

- WRONG DATA COMPARE: message used by both floppy and minifloppy to indicate that the data string loaded and subsequently read in memory has been altered with regard to its original contents.

- UNIDENTIFIED DISK: (FDU) disk loaded does not conform to formatting standards as defined by standard 24.

- DEFECTIVE TRACK ASSIGNATION: (FDU, step 100) initialization command for defining defective tracks and assigning alternative tracks.

- HOME COMMAND: (FDU, step 101) reset command for positioning the read/write head.

- MODE ASSIGN: (FDU, step 102) initialization command to establish the operating modes.

- READ PREDISPOSITIONS COMMAND: (FDU, step 103) read command issued during preprogramming stage to obtain data needed for initialization.

- FDU START I/O COMMAND: (FDU, step 104) initialization command for IOCB which determines type of operations to be performed (i.e. read/write). This command is normally issued during overlapping operations.

- FDU END I/O COMMAND: (FDU, step 105) command to indicate end of IOCB. This command is also used during overlapping operations.

- KEYBOARD 0 ACTIVATION COMMAND (RC=....): (keyboard, step 110 and 111) command to activate transmission of characters to/from keyboard (set/reset, shift lock indicator). RC register contains information on error causing the malfunction.

- START KEYB 0 RECEIVE COMMAND (RC=....): (keyboard, step 112) start overlap command for character reception. RC contains the command issue response

- START KEYB 0 RECEIVE COMMAND (RC=....): (keboard, step 113) end of character reception. RC contains the command end response.

- TEST MONITOR 0 COMMAND (RC=...): (video, step 120) to acquire information on the type of video connected. RC contains the end conditions.

- UNIDENTIFIED MDISK: (MFD) disk loaded does not conform to formatting specification as defined in standards 24.

- DEFECTIVE TRACK ASSIGNATION: (MFD, step 130) initialization command for defining defective tracks and assigning alternative tracks.

- HOME COMMAND: (MFD, step 131) reset command for positioning the read/write head

- MODE ASSIGN: (MFD, step 132) initialization command to establish the operating modes

- READ PREDISPOSITIONS COMMAND: (MFD, step 133) read command issued by the preprogram to obtain data needed in initialization

- MFDU START I/O COMMAND: (MFDU, step 134) initialization command for IOCB which determines type of operations to be performed (i.e. read/write). This command is normally issued during overlapping operations.

- MFD END I/O COMMAND: (MFDU, step 135) end of command for IOCB.

- PRINTER 1: START WRITE COMMAND (RC=....): (printer 1, step 140) command in overlap issued. RC contains the response

- PRINTER 1: END WRITE COMMAND (RC=....) (printer 1, step 141) end of print command. RC contains the command end response.

4.7 ENCDES: CLOCK & ENCRYPTION (NON SEGMENTED) TEST PROGRAM

PROGRAM PURPOSE

To test the ENCRYPTION and REAL TIME CLOCK controller.

HARDWARE REQUIRED

ENCRYPTION/DECRYPTION controller (type 21 with PKAC EPROM).

LOADING PROCEDURES

Refer to section 1.3.2

NOTE

This program cancels all the encryption parameters, including the MASTER KEY code in Key RAM. The program does not permit writing in the NOVRAM (EAROM) but the NOVRAM may be written to as a result of an error.

GENERAL

The tests in this program must be carried out in sequential order, therefore individual tests must NOT be omitted as any modification of the test sequence will affect results.

Tests 1 to 6 can be repeated a number of times but tests 7 to 11, relating to the controller Encrypt/Decrypt section must NOT be repeated (even after RESET) as an error may cause a write operation in the NOVRAM and thus reduce its life expectancy.

Tests can be limited to tests 1 to 6 by entering 1 (=no) when replying to the prompt "DO YOU KNOW THE PASSWORD VALUE".

Particular care should be taken in entering the passwords and the offset, remembering that the ENTER and not the RETURN key is to be hit after entering the last digit of each code.

Initially when requested to retype password the system should be tested by deliberately entering an incorrect password and then verifying that program returns to its original request.

After testing, the modified contents of the Key RAM should be removed by taking the board out of the slot or by lifting off the battery supply plug, WITH THE SYSTEM OFF. When switched on again, the Key RAM will be re-initialized by the firmware.

WARNING

IF IT IS KNOWN THAT AN INCORRECT CODE HAS BEEN ENTERED TWICE THEN THE SYSTEM MUST BE RESET.

NOTE (2)

The password used in production comprises a series of noughts. This is modified by the end user on site.

4.7.1 TEST DESCRIPTION

TEST 1: ENCRYPTION SLOT TEST

Checks that the slot corresponding to the number entered by the operator in the pre-program contains the correct controller. The 8 most significant bus bits are checked to see if they read "FF".

Note : When signals 1AD10, 1AD20 or 1AD30 are at "0", it should not be possible to read the board type.

TEST 2: VERIFY FLAGS ON DUAL PORT MEMORY

Checks that the Encryption/Decryption controller emits "free" signal after the power-on autodiagnostic tests. The diagnostic status in the Dual Port Memory response area is then read and the appropriate error message displayed if there are errors.

TEST 3: DUAL PORT MEMORY TEST

Checks the Dual Port RAM and relative scatter logic. After verifying that the Dual Port RAM is present, the arbitration circuit handling memory requests and byte/word addressing selection is checked.

Checks instantaneous reading/writing operation of the Dual Port RAM. The entire RAM is written to without interruption; any incorrect data or addresses are detected in the subsequent memory read.

The Nair, Thatte and Abraham test algorithm, in reduced version, is then run. Though not as comprehensive as the full version, execution time of the reduced version is considerably shorter.

Signal MEGON should not be output at memory addresses which do not select the Encryption controller. Finally, the Dual Port RAM diagnostic command is checked.

TEST 4: SPECIAL INTERRUPT TEST

Checks the operation of the interrupt logic using the "set special interrupt" command.

TEST 5: INTERRUPT VECTOR BUFFER TEST

Checks the interrupt vectors on the relative gates, and consequently, the vectors themselves.

TEST 6: REAL TIME CLOCK

Checks the clock stop command; the correct time and data parameters are entered and then incorrect parameters entered and the responses checked. The correct parameters are then re-entered.

The clock operation is then released after the correct time parameters are loaded and the time parameters checked.

TEST 7: SECONDARY PASSW. TEST

Checks the new secondary passwords entered in Key RAM. The secondary password currently in the Key RAM is compared with the one in the program field.

This field may be the one entered by the operator, in cases where the board already has a password other than 0, or a number of zeroes if the operator simply hits ENTER where the board has no secondary password.

The controller loses the secondary password when:

1. the board is removed from the rack

2. the system is off and the plug supplying the Key RAM through the board batteries is removed

3. the board is new

A new secondary password is written into Key RAM and checked; the original secondary password is then re-entered. The test is carried out if it has been stated in the preprogram that the operator does not know the passwords.

TEST 8: PRIMARY-OFFSET PASS. TEST

Checks the primary and offset passwords. Incorrect configurations are not tested to avoid incrementing the NOVRAM error counter EACOUNT and thereby shorten its life (approximately 1000 write operations).

The DCP deciphers the primary and offset passwords in ECB before recording them and comparing them with those in NOVRAM.

TEST 9: MASTER KEY TEST

The master key is loaded in the Key RAM. The contents of the master key are then cancelled. When the offset is not 0, the program ensures that the master key cannot be loaded if the primary password has not been checked; the master key is then re-loaded without a parity check.

TEST 10: CRYPTOGRAPHIC PARAMETER TEST

The Encryption/Decryption parameters are first loaded and then those with identifiers from 01 to 7F are cancelled. If the offset is other than 0, with similar password and offset, the test also checks that the "mid" and "ID" responses are the same as before.

A check is also made to see that characters already encrypted are correctly loaded.

TEST 11: ENCRYPT./DECRYPT. TEST IN CF MODE

After the Master Key and encryption parameters are loaded in Key RAM, a text encryption operation is issued in CF mode, and the results are checked. The encrypted text is then input to the ERU controller for decryption. The resulting text is compared with the text originally presented for encryption to check CF mode operation.

FAULT FINDING HINTS

If a specific error occurs in tests 2 to 6 the help routine can be accessed to repeat certain tests in order to investigate the fault.

If an INTERVAL TIMER NOT GO OUT error is indicated, check for 5.1 volts on the power supply terminals.

The Real Time Clock can be checked by setting a probe on the test point in position B10; if the clock is not working the output at this point, (signal SEC00) remains fixed.

If an NMI (Non Maskable Interrupt) is generated during the program, check if signal LESVA is fixed at 0.

If the program cannot be loaded from floppy disk and/or the system does not accept commands, see if signal INPN0 is stuck at 1.

If the program stops during test 4 (Special Interrupt) and no error message displayed, check for signal DAST2 stuck at 0 or 1 and signal INUS0 at 0.

For a "RAM A08: BIT 7 STUCK 1 (BUSY)" error message, check for one of the following conditions:

MASTB stuck at 1, OKMEO stuck at 0
TEBUO stuck at 0, ZEWAN stuck at 0
ZECL2 stuck at 1/0, ZWRIT stuck at 1
ZREAD stuck at 1, IOREQ stuck at 1/0
CEROA stuck at 1/0, ZERON stuck at 1

4.7.2 ERROR AND SERVICE MESSAGES

The error messages displayed are listed below with notes:

- *** PRIVILEGED INSTRUCTION TRAP ***

  indicates that a privileged instruction has been executed in user mode.

- *** SEGMENT TRAP ***

  indicates that a memory segment not handled by the MMU has been accessed.

- *** NON MASKABLE INTERRUPT ***

  a non-maskable interrupt has been generated, this is usually followed up by a 4 figure number, in which the first two figures represent the test number and the last two the error number.

- ANSWER TO BOARD TYPE HAS VALUE = FF

- BOARD TYPE DIFFERENT TO EXPECTED VERIFY IF BOARD IS INTO SLOT
  ASSIGNED OLIBUS SIGNAL READS BY INPUT INSTRUCT.
  READ BOARD TYPE XX
  IDAYO STUCK AT Z

  here, XX is the controller type read, Y the incorrect bit number and Z is either 0 or 1.

- 8 BIT + SIGNIF. DATA BUS DO NOT = FF

- indicates that the most significant data bus bits are not at 1.

- XXXX = YYYY COMPLEM. SELECT BOARD

  where XXXX = ADA11, ADA12, ADA13, ADA14 or ADA15
  and YYYY = NOXLA, NOSL0, NOSL1, NOSL2 orNOSL3

  indicates that the controller is selected when XXXX = YYYY complemented.

- IAD10 = 0 SELECT BOARD TYPE

- IAD20 = 0 SELECT BOARD TYPE

- OUTPUT OF RESET BLOCKS BOARD TYPE

- ON THIS SLOT IT IS NOT THE BOARD

- indicates that the controller board is not in the slot entered in the pre-program

- IAD30 = 0 SELECT BOARD TYPE

- SLOT POSITION DO NOT POSSIBLE

  indicates that the slot number entered in the pre-program does not exist

- ERROR CODE DO NOT EXPECTED IN TEST

  indicates that the error code found is not known.

- BOARD TYPE DIFFERENT TO EXPECTED OLIBUS SIGNALS READS BY
  INPUT INSTRUCT.
  READ BOARD TYPE XX
  1DAY0 STUCK AT Z

  here, XX is the controller type read, Y = incorrect bit no. and Z is either 0 or 1.

- RAM A08: ADDR. = 000, BIT 6 STUCK 1

- RAM A08: BIT 7 STUCK 1 (BUSY)

- RAM A08: ADDR = 021 ANSW. NOT CORRECT 0
  VERIFY WRMEN ST.1 - MAD50 - MAD10 ST.0/1

  indicates that the program has not responded correctly; the signals quoted may be stuck

- BLOCK ERROR: CRC ROM FIRMWARE (B09)

- BLOCK ERROR: STACK POINTER IN K.RAM - G09

  where K = Key

- BLOCK ERROR: COMAND AREA IN D.P. RAM - A08

  where D.P. = Dual Port

- RAM A08: ADDR. = 22 - 23, SINDROME STUCK 00

- RAM: FT = 0, ANSW. CODE = 0 BUT BLOCK BIT 0
  VERIFY IF MAD00 ST.0/1

- VERIFY: RAM A08 OR ITS SELECTION

- NO WRITE RAM DUAL PORT FROM Z80

  indicates that the Z80 write Dual Port RAM operation has not taken place

- ERROR ON WRITE FROM Z80 IN RAM A08

- SEL. RAM A08 ERROR, READS FF: OEMEN, CSDUE

- VERIFY: DATA/ADDR. BUS FROM Z80, OR Z80

- VERIFY: RAM A08, MAD0 - A0, MDA0 - 70

- INTERRUPT (NMI) NOT EXIT AT THE RESET

  indicates that the NMI interrupt has not been generated on controller reset

- WR BYTE WRITE SAME CELL: MDA00 - RAM A08

  indicates the same cell has been over written in a byte write operation

- WR ODD BYTE MODIFY EVEN BYTE TOO: RAM

  indicates that even bytes are also modified in an odd byte write operation

- ODD DATA BUS PASS IN WORD WRITE: MENON

  indicates that a word write operation has been performed with odd data bus

- TESTED ADDR. 040 - 041 OF RAM
  ERROR ON WORD WRITE:RAM A08
  READ: XXXX EXPECTED: YYYY

  here XXXX = actual data read and YYYY = data expected

- WORD WRITE APPROACHED NEXT CELL TOO

- ERROR ON RAM CELL (A08)

- ADD: XXXX READ: YYYY EXPECTED: ZZZZ

- ERROR ON ADDRESS MAD0/A0 OF RAM A08
  WRITE ADDR. 1 WROTE ADDR. 2 TOO
  ADD 1: XXXX ADD 2: YYYY

- ERROR ON RAM CELL (A08)
  READ: XXXX EXPECTED: YYYY

- ERROR ON ADDXX

- ERROR ON NOSLX OR ADDXX

- NOT RD AT SLOT = XX, WITH ADD15 INVERT.

- RD AT SLOT XX, WITH ADD15 INVERTED

- ERROR ON DUAL PORT RAM (A08)
  ADD: XXXX

- EVEN DATA BUS OR ADDRESS OR RAM A08

- NOT ENABLE EVEN DATA BUS (B02): PIUON
  indicates that even data bus cannot be enabled; investigate signal
  PIUON

- RAM A08, NOT PRESENT OR NOT SELECTED
  VERIFY OEEN ST.1 - CSDUE ST.1

- TESTED ADDR. 040 - 041 OF RAM
  VER.: WRMEN, ODD DATA BUS, RWGOA, RAM A08
  READ:XXXX EXPECTED:YYYY

- TESTED ADDR. 040 - 041 OF RAM
  ERROR ON ADA8/15 OR RAM CELL (A08)
  READ:XXXX EXPECTED:YYYY

- TESTED ADDR. 040 - 041 OF RAM
  ERRON ON MDA00/70 OR RAM OR DMAK0
  READ:XXXX EXPECTED:YYYY

- TESTED ADDR. 040 - 041 OF RAM

- TRANSC. B05 - B03 ODD DATA BUS, OR RWGOA
  READ:XXXX EXPECTED:YYYY

- TESTED ADDR. 040 - 041 OF RAM
  1DA0/70 OR HIS TRANSC. B05 OR RAM A08
  READ:XXXX EXPECTED:YYYY

- ERROR ON D.P. RAM A08: VERIFY B50 - 70
  FROM Z80 AND PORT B07

- Z80 CPU DO NOT PUT BUSY = 0 IN RAM A08

  Busy is not set 0 in RAM A08

- ERROR ON CIRCUIT WHICH SELECT ACCESS TO
  DUAL PORT MEMORY BY Z80 OR Z8000
  ERROR ON WRITE BY Z80
  VERIFY F.F. L06, B06, DMAK0 - CEBU0 - RAM0C

- ERROR ON CIRCUIT WHICH SELECT ACCESS
  TO DUAL PORT MEMORY BY Z80 OR Z8000
  ERROR ON WRITE BY Z8000
  VERIFY F.F. L06, B06, DMAK0 - OKZ00 - ASP00

- V.I. UNEXPECTED: VINTA, LESVA, INPN0, 1E1X0

- Z80 DO NOT MOVE BIT - IP - CORRECTLY

- NOT GO OUT V.I.: VINTA, LESVA, INPN0, 1E1X0

- ERROR ON VECTOR TRANSM. PORT (B04)
  VERIFY IF CK LESVA WHEN BS00 - 70 VALID
  VECTOR OK:%XXXX VECTOR KO:%YYYY

  here, XXXX is the correct vector number, YYYY = the incorrect number

- ERROR CODE DO NOT EXPECTED IN TEST

  indicates that an incorrect code has been found

- CPU SLAVE Z80 DO NOT PUT BUSY = 0

- ERROR ON VECTOR TRANS. PORT (B04)
  VECTOR OK:%XXXX VECTOR KO:%YYYY

- CPU SLAVE Z80 COMPILE WRONG ANSWER

- R.T.CLOCK (P.B.B09) NOT EVOLVES:VERIFY
  CLOCK B09, QUARTZ A10, CERTM, ZEROZ, TEBUO

  indicates that the Real Time clock is not working

- FIRMW. OR Z80 NOT EXECUTE STOP CLOCK

  firmware or Z80 cannot stop the clock

- PARAMETER OK, FIND KO BY Z80 OR FIRMW

  indicates that the parameters are OK, but operation is faulty

- PARAMETER KO, FIND OK BY Z80 OR FIRMW

  indicates parameters faulty and operation OK

- R.T.CLOCK (B09): SECONDS NOT EVOLVES

  indicates that the Real Time clock does not increment in seconds

- R.T.CLOCK (B09): SECONDS EVOLVES NOT
  CORRECTLY - VER. QUARZ OR CLOCK DATA BUS
  READ:XXXX EXPECTED:YYYY

- R.T.CLOCK (B09): MINUTES NOT INCREASE
  READ:XXXX EXPECTED:YYYY

  indicates that the Real Time clock does not increment in minutes

- R.T.CLOCK (B09): HOURS NOT INCREASE
  READ:XXXX EXPECTED:YYYY

  indicates that hours of the Real Time clock does not increment

- R.T.CLOCK (B09): DAYS NOT INCREASE
  READ:XXX EXPECTED:YYYY

  indicates that the days of the Real Time clock does not increment

- R.T.CLOCK (B09): MONTHS NOT INCREASE
  READ:XXXX EXPECTED:YYYY

  indicates that the months of the Real Time clock does not increment

- R.T.CLOCK (B09): YEARS (BYTE+) INCREASE
  READ:XXXX EXPEXTED:YYYY

  indicates that the most significant months of the Real Time clock does not increment

- R.T.CLOCK B09: YEARS (BYTE-) NOT INCREASE
  READ:XXXX EXPECTED:YYYY

  indicates that the least significant months of the Real Time clock does not increment

- R.T.CLOCK B09: MINUTES NOT GO BACK TO 0
  READ:XXXX EXPECTED:YYYY

  indicates that the minutes of the Real time clock does not decrement

- R.T.CLOCK (B09): HOURS NOT GO BACK TO 0
  READ:XXXX EXPECTED:YYYY

  indicates that the hours of the Real time clock does not decrement

- R.T.CLOCK (B09): DAYS NOT GO BACK TO 01
  READ:XXXX EXPECTED:YYYY

  indicates that the days of the Real time clock does not decrement

- R.T.CLOCK B09: MONTHS NOT GO BACK TO 01
  READ:XXXX EXPECTED:YYYY

  indicates that the months of the Real time clock does not decrement

- INTERVAL TIMER NOT GO OUT: KEY RAM (G09)

  indicates that the interval timer is not generated

- VECTORED INTERRUPT WITH VECTOR DIFFER.
  TO: VECTOR +2 DURING TIME DEDICATE TO
  INTERRUPT FOR INTERVAL TIMER TERMINATE
  VECTOR READ:XXXX EXPECTED:YYYY

- KEY RAM: INTERVAL TIMER ORDER END
  FOUND NOT CORRECT (P.P. G09)

- INTERVAL TIMER WITH IDENTIFIER
  XXXX NOT GO OUT

  indicates that the Interval timer with identifier XXXX is not generated

- INTERVAL TIMER IDENTIFIER IS NOT CORRECT
  READ:XXXX EXPECTED:YYYY

- INTERRUPT OF END CYCLE NOT GO OUT
  ON COMMAND OF LOAD INTERVAL TIMER DATA

- NOVRAM CRC ERROR (E07)
  VER. RESEA - CEWRA - ZA0/50 - CESTA - ZEWRN
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES
  VERIFY CERTN STUCK 0/1

  indicates a NOVRAM CRC error; the program cannot continue

- KEY RAM ERROR (G09)
  VER. CERAA - ZEROZ - TEBU0 -ZA0/100
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES

- CTC CHANNEL DO NOT INCREASE (M09)
  ZECL2 - ZERON - CECRA - ZEM1N - ZA0/10 - SEC00
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES

  indicates that the CTC channel does not increment

- REAL TIME CLOCK: NOT INCREASE MICROSEC
  VER. TEBU0 - OSCIN - CERTN - ZERDZ - ZA0/40
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES

  indicates that the microseconds does not increment

- DCP ERROR (D08)
  VER. 2MHZ0 - RZA00 - ZEASA - ZEDSA - CEDCA
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES

- MAX NUMBER ERRORS FOR PWD. NOVRAM - E07
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES

- MAX NUMBER ERRORS FOR PWD. SECOND. - G09
  DIAGNOSTIC PROGRAM CANNOT GO BESIDES

- RAM P.G09 OR ZERDZ - CERAZ - ZEWRZ - TEBU0

- RAM P.G09: KEYCOUNT FAILED (=256 = MAX)

  indicates faulty counter

- RAM P.G09: NO MATCH PASSW. SECONDARY

  indicates that the secondary password does not correspond

- RAM P.G09: KEYCOUNT FAILED   0

- RAM P.G09: KCOUNT DO NOT COME BACK TO 0

- RAM (G09): KCOUNT NOT INCREASE CORRECT

- RAM P.G09: ZEWRZ (NO WRITE IN MEMORY)

- RAM P.G09: KEYCOUNT DO NOT INCREASED

- RAM P.G09: CONTAIN NOT CORRECT
  PARAMETERS OF PASSWORD SECONDARY
  VERIFY ALSO BSO - 70 END ZA0 - 100

- Z80 CPU DO NOT PUT BUSY=0 W RAM A08

- ERROR CODE DO NOT EXPECTED IN TEST

- CRC NOVRAM P.P.E07: CEVRA - RESEA - ZA0 - 50

- NOVRAM P.P.E07: EACOUNT = MAX (256)

- OO NOT KNOW PASSWORD PRIMARY OK
  NOVRAM P.P.E07 OR DCP P.P.D08 OR THESE
  SIGNALS AROUND THE DCP: RZA00 -
  ZEASA - ZEDSA - CEDCA - AUASA - 2MHZO

  Primary password not recognised

- NOVRAM P.P.E07: EACOUNT FALLED 0

- DO NOT KNOW PASSWORD OFFSET OK
  NOVRAM P.P.E07 OR DCP P.P.D08 OR THESE
  SIGNAL AROUND THE DCP: RZA00 -
  ZEASA - ZEDSA - CEDCA - AUASA - 2MHZO

- KEY RAM P.P.G09: ZA0 - 100, CERAZ
  ZERDZ, ZEWRZ

- NO ACKNOWLEDGE PASSW. PRIMARY WHEN OK
  NOVRAM P.P.E07 OR DCP P.P.D08

- LOAD M.KEY WITHOUT VERIFY PWD. PRIMARY

- FIRMWARE DO NOT ACCEPT - NDM - = 0

- DIAGNOSTIC CODE NOT PREVIOUSLY

  code not accounted for

- DCP P.P.D08: MISMATCH ON PARITY CHECK

- FIRMW. DO BIT ACCEPT PARAMETER AND
  SIGNS PWD. OFFSET NOT VERIFIED ALSO
  WHEN THIS PASSWORD WAS BEEN VERIFIED

- PARAMETER OK NOT ACCEPTED
  VERIFY ROM (B09) - Z80 (D10)

- MID (MASTER KEY ORDER NUMBER) IS 0
  INTO ANSWER BY Z80

- IDENTIFIER COMPILED BY Z80 INTO
  ANSWER IS DIFFERENT TO EXPECTED
  VERIFY ROM (B09) - Z80 (D10)

- ATTRIBUTE COMPILED BY Z80 INTO
  ANSWER IS DIFFERENT TO EXPECTED
  VERIFY ROM (B09) - Z80 (D10)

- BYTE OF ATTRIBUTE CIPHERED BCB NOT
  CORRECT: VERIFY DCP (P.P.D08)

- BYTE OF ATTIBUTE CIPHERED BCB NOT =
  TO BYTE IN KEY MEMORY: RAM (G09)

- FIRMW. DO NOT ACCEPT PARAMETER AND
  SIGNS PWD. SECONDARY NOT VERIFIED ALSO
  WHEN THIS PASSWORD WAS BEEN VERIFIED

- ATTRIBUTE CIPHER ECB NOT CHANGED BY
  DIFFERENT MASTER KEU WHEN OFFSET 0
  VERIFY NOVRAM P.P.E07, OR DCP P.P.D08

- AUTODIAG. ERROR: PARAMETER OF KEY RAM
  FOUND INCORRECT RESET AND REPEAT

- RAM G08 FAILED: CELL - ID - OF PARAMETER
  CONTAIN - ID - DIFFERENT TO EXPECTED

- DCP NOT PROGRAMMED CORRECTLY
  VERIFY DCP AND HIS SELECTIONS

- FIRMW. SIGNS PARAMETER OF ENCRYPTION
  FAILED WHEN OK (OFFSET + BLOCK LENGHT)

- ERROR ON DECRYPTION IN "CF" MODE
  VERIFY DCP (P.P.D08)

- INTERRUPT (NMI) NOT EXIT AT THE RESET
  NMI not generated on controller reset

- ** DIAGNOSTIC RESULT: HARDWARE FAULT **

  a summary message indicating that at least one error has been found

4.8 ENCSEO :ENCRYPTION CONTROLLER (SHARED SEGMENT) TEST PROGRAM

PROGRAM PURPOSE

To test the Encryption/Decryption and Real Time Clock controller.

HARDWARE REQUIRED

Video/keyboard controller, floppy disk unit controller, ENCRYPTION/DECRYPTION controller (type 33 with PKAC EPROM).

LOADING PROCEDURES

Refer to section 1.3.2

NOTE (1)

This program cancels all the encryption parameters, including the MASTER KEY code in Key RAM. The program does not permit writing in the NOVRAM (EAROM) but the NOVRAM may be written to as a result of an error.

GENERAL

Refer to the correspondong section in the ENCDE5 program (section 4.9).

NOTE

The password used in production comprises a series of noughts. This is modified by the end user on site.

4.8.1 TEST DESCRIPTION

See corresponding sections of the ENCDE5 program for test description (para. 4.9.1) and list of error messages (4.9.2).

4.9 PINCK1: PIN CHECK ENCRYPTION CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To check the PIN ENCRYPTION/DECRYPTION controller.

HARDWARE REQUIRED

Video/keyboard controller, floppy disk controller, ENCRYPTION/DECRYPTION controller, PIN CHECK version (type 33 with PKAD/PKAH EPROM).

LOADING PROCEDURES

Refer to section 1.3.2

NOTE (1)

This program cancels all the encryption parameters, including the MASTER KEY code in Key RAM. The program does not permit writing in the NOVRAM (EAROM) but the NOVRAM may be written to as a result of an error.

GENERAL

Refer to the corresponding section of the ENCDE5 program (section 4.9).

WARNING

IF IT IS KNOWN THAT AN INCORRECT CODE HAS BEEN ENTERED TWICE THEN THE SYSTEM MUST BE RESET.

NOTE (2)

The password used in production comprises a series of noughts. This is modified by the end user on site.

4.9.1 TEST DESCRIPTION

Refer to corresponding sections of the ENCDE5 program for test description (para. 4.9.1).

Test 1 through to test 6 are identical.

Test 7 (PRIMARY-OFFSET PASS TEST) of this program is described in test 8 of the ENCDE5 program.

Test 8 (MASTER KEY TEST) of this program is described in test 9 of the ENCD5 program.

Tests 9 and 10 are not the same and are therefore described below:

TEST 9: PIN-CHECK TEST IN-IPACRI-MODE

A total diagnostic command is issued to have a PIN check made in IPACRI mode. As the master key must be at 0 for this, it is reset at the beginning after the primary password has been checked. The PIN check parameters, including those entered by the customer (relating to the badge and keyboard), are loaded and a check made that the controller acknowledges error conditions on the input parameters in the PIN check process.

TEST 10: PIN-CHECK TEST IN-COMIT-MODE

A diagnostic command is issued to have a PIN check made in COMIT mode. As the master key must be at 0 for this, it is reset at the beginning after the primary password has been checked. The PIN check parameters, including those entered by the end user (relating to the badge and keyboard), are loaded and a check made that the controller acknowledges error conditions on the input parameters in the PIN check process.

4.9.2 ERROR MESSAGES

The error messages are the same as listed in the ENCDE5 program (sect. 4.9.2) with the addition of the following:

- COMMAND START ENCRYPTION FALSE
  (FOR PIN-CHECK ACKNOWLEDGEMENT)

- WARNING: BOARD UNDER TEST IS
  ENCRY/R.T. CLOCK INSTEAD OF PIN-CHECK

- ERROR IN WR PARAMETER FOR PIN-CHECK

- IN D.P.RAM ALREADY TESTED : RAM P.A08

- FIRMW. SIGNS M.KEY NOT PRESENT WHEN
  THE M.KEY = 0 :ROM P.B09 OR DCP P.D08

- ERROR IN PIN-CHECK (IPACRI MODE): DIAGN.CODE FROM Z80 NOT EXPECTED:ROM

- VERIFY DCP P.D08 OR KEY RAM P.G09

- (IPACRI MODE),NOT CORRECT.WHEN OK:DCP

- ERR. IN DIAGN.START COMMAND (LED ON):

- VERIFY DCP P.D08

- FIRMW. SIGNS PIN-CHECK IPACRI MODE=OK

- ALSO WITH PARAM. -CHLEN- WRONG (=0)

- ALSO WITH WRONG PARAM. : MAXPIN<CHLEN

- ALSO WITH WRONG PARAMETER -LVALDATA-
- FIRMW. NOT CLEAR PARAMETER AREA INTO
- D.P.RAM AFTHER PIN-CHECK COMMAND:ROM
- ERROR IN PIN-CHECK (COMIT MODE):
- DCP P.D08 NOT OK
- R.T.CLOCK P.B09 NOT OK
- CTC P.M09 NOT OK
- KEY RAM P.G09 NOT OK
- D.P.RAM P.A08 NOT OK
- NOVRAM P.E07 CRC NOT OK
- (COMIT MODE),NOT CORRECT.WHEN OK:DCP
- FIRMW. SIGNS PIN-CHECK COMIT MODE =OK
- 1DA = XXXX

4.10 COENC2: ENCRYPTION (SHARED SEGMENT) TEST PROGRAM - FOR PNS2197 OR DEM8038

PROGRAM PURPOSE

To test the Encryption/Decryption and Real Time Clock controller for PNS2197 or DEM8038.

HARDWARE REQUIRED

Video/keyboard controller, floppy disk unit controller, ENCRYPTION/DECRYPTION controller for PNS2197 or DEM8038.

LOADING PROCEDURES

Refer to section 1.3.2

NOTE

This program cancels all the encryption parameters, including the MASTER KEY code in Key RAM. The program does not permit writing in the NOVRAM (EAROM) but the NOVRAM may be written to as a result of an error.

GENERAL

The tests in this program must be carried out in sequential order, therefore individual tests must NOT be omitted as any modification of the test sequence will affect results.
Tests 1 to 6 can be repeated a number of times but tests 7 to 11, relating to the controller Encrypt/Decrypt section must NOT be repeated (even after RESET) as an error may cause a write operation in the NOVRAM and thus reduce its life expectancy.
Tests can be limited to tests 1 to 6 by entering 1 (=no) when replying to the prompt "DO YOU KNOW THE PASSWORD VALUE".
Enter the passwords and the offset, remembering that the ENTER and not the RETURN key is operated after entering the last digit of each code.
Initially when requested to retype password the system should be tested by deliberately entering an incorrect password and then verifying that program returns to its original request.
After testing, the modified contents of the Key RAM should be removed by taking the board out of the slot or by lifting off the battery supply plug, WITH THE SYSTEM OFF. When switched on again, the Key RAM will be re-initialized by the firmware.

WARNING

IF IT IS KNOWN THAT AN INCORRECT CODE HAS BEEN ENTERED TWICE THEN THE SYSTEM MUST BE RESET.

NOTE

The password used in production comprises a series of noughts. This is

4.10.1 TEST DESCRIPTION

Refer to test description of the ENCDE5 program described in section 4.7.2.

4.10.2 ERROR MESSAGES

Refer to error messages of the ENCDE5 program described in section 4.7.3.

4.11 ERTC01: ENCRYPTION ONLY REAL TIME CLOCK TEST PROGRAM

PROGRAM PURPOSE

To check the ENCRYPTION controller, "only Real Time Clock" version.

HARDWARE REQUIRED

Video/keyboard controller, floppy disk controller, ENCRYPTION controller, "only Real Time Clock" version.

LOADING PROCEDURES

Refer to section 1.3.2

NOTE

This program cancels all the encryption parameters, including the MASTER KEY code in Key RAM. The program does not permit writing in the NOVRAM (EAROM) but the NOVRAM may be written to as a result of an error.

GENERAL

The tests in this program must be carried out in sequential order, as any modification of the test sequence will affect results.

Tests can be repeated a number of times.

The password used in production comprises a series of noughts. This is modified by the end user on site.

4.11.1 TEST DESCRIPTION

Refer to test 1 through to test 6 of the ENCDE5 program described in section 4.7.2.

4.11.2 ERROR MESSAGES

Refer to error messages of the PINCK3 program described in section 4.9.3.

4.12 CESTEO: EXTENDED CONSOLE FOR M64/M70 TEST

PROGRAM PURPOSE

This program is designed to check correct operation of the extended console and the communication lines between the master CPU and console and between the console and slave CPUs.

HARDWARE REQUIRED

Extended console, CPU board UC070 (for M64), or from one to three UC071 CPU boards (for M70), RAM board.

N.B.: From this point on, the term **display** will be used to refer to the 6-character, alphanumeric display on the console and the term **video** for the monitor of the workstation from which the tests will be run.

LOADING PROCEDURES

Refer to section 1.3.2.

4.12.1 TEST DESCRIPTION

1. **FUNCTIONAL TEST**

   This test checks that the hardware of the extended console is in correct working order by running a series of tests on all the devices.

   - **CONSOLE STRUCTURE.** The console configuration and firmware release are checked, an autodiagnostic test run on the console and the "echo" function checked.

   - **DISPLAY MANAGEMENT.** Six hexadecimal characters (figures 0 to 9 and letters A to F) are entered by the operator their display on the display is confirmed and then the following cyclic pattern of 32 characters is displayed:

     1111 2222 3333 4444 5555 6666 7777 8888.

     The display is confirmed to be off; then the following character patterns are displayed:

     "555AAA", "AAA555" and "000000".

     The operator checks that the correct characters are displayed

   - **LED NO-GO MANAGEMENT.** The NO-GO LED on the front panel of the console is first switched off, then made to blink, switched on and then off again.
     The operator checks that the LED behaves correctly.

- **BUZZER MANAGEMENT.** The operator checks that the buzzer operates correctly.

- **RTC MANAGEMENT.** A menu to be followed in performing the operations listed below is displayed:

  . Completely re-program the Real Time Clock, setting, in order, the type of calender (Gregorion or Showa) and year, the month, day of the month, day of the year, type of time (a.m., p.m., or 0-23), hour, minutes and seconds.

  . Show hour and minutes on display or cancel display.

  . Partly re-program the Real Time Clock setting, in order, the day of the week, year, month, day, hour, minutes and seconds or only the hour, minutes and seconds.

  . Enable and disable the Real Time Clock to perform the restart and/or the automatic reset, setting the parameters required.

  . Enable and disable the SET SYS ON function (automatic switch-on) for each day of the week and display the status.

- **CONSOLE INFORMATION.** Console status information, listed below, is supplied:

  . System switch-on method: KEY= manual, LINE= remote, TIMER= automatic.

  . Key position: RUN or STAND-BY.

  . ISL device selected: ISL 1-A, ISL 1-M or ISL 2.

  . Status of the DUMP, EXDIA and FIRMWARE MODE functions: ON or OFF.

- Reset or display the ERROR LOGGING registers: ALIUP, DATE, FAN-FAIL and POWER UP.

- Perform or otherwise the system reset.

- Enable or disable the automatic reset and/or the "unattended" condition.

2. **MULTIPROCESSOR TEST**

   This test checks correct operation of the communication lines between the Master CPU and console and the console and the slave CPUs (where present).

4.12.2 ERROR MESSAGES

- INCORRECT UC MASTER SLOT NUMBER
- SLAVE #1 NOT READY
- SLAVE #2 NOT READY
- MODE
- TARGET CPU NOT PRESENT
- TARGET CPU DOES NOT ACKNOWLEDGE
- TARGET CPU NOT READY
- TARGET NAME SAME AS SOURCE
- TRANSMISSION ERROR
- RECEPTION ERROR
- ANSWER NOT EXPECTED ERROR
- ANSWER CODE ERROR
- REAL TIME CLOCK NOT PROGRAMMED
- AUTOMATIC RESTART TIMER NOT PROGRAMMED
- AUTOMATIC RESET TIMER NOT PROGRAMMED

4.13 SSM000: EXTENDED CONSOLE WITH TEDIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To check the extended console whit telediagnostic operation and the communication lines between the console and Slave CPU's.

HARDWARE REQUIRED

Extended console with telediagnostic (SSM), CPU board UC070 (for M64), or from one to three UC071 CPU boards (for M70), RAM board.

N.B.: From this point on, the term **display** will be used to refer to the 6-character, alphanumeric display and the term **video** for the monitor of the workstation from which the tests will be run.

LOADING PROCEDURES

Refer to section 1.3.2.

4.13.1 TEST DESCRIPTION

Refer to test description of CESTE0 program described in section 4.12.2.

4.13.2 ERROR MESSAGES

Refer to error messages of CESTE0 program described in section 4.12.3.

4.14 PCA100: CA2000/2020 IN CU, ELB1382 AND TWIN CONNECTION

PROGRAM PURPOSE

To check operation of the CA2000 (or CA2020) and physical and logical connection to the CU, ELB1382 or TWIN.

HARDWARE REQUIRED

CA2000 or CA2020 unit. Optionals: ELB1382 and TWIN controller.

WARNING

- The parameters entered by the operator must correspond to those of the CA2000. If they do not, errors will be signalled which are not the result of CA2000 malfunctions. The CA2000 may be programmed with the 16-position rotary DIP-switch SW3 (DIP-switch SW2 must be kept open).

- If tests 4 and 5 are not carried out in the default sequence, they must be performed after test 3; otherwise, an error is reported.

- If the connection is via ELB1382 or TWIN, a 50 second timer is set off before all I/O operations, so that if nothing of significance occurs, wait until after the time-out for information.

LOADING PROCEDURES

See section 1.3.2.

4.14.1 TEST DESCRIPTION

GENERAL

At the end of each test, status indication reports (warning and/or error) are given in complete message form. Any one of the tests may be left out and all may be repeated.

TEST 1 - CA2000 CONNECTION

Checks hardware connection of the CA2000 to the system board connected (CU/TWIN/ELB1382).

TEST 2 - RESET

Resets the CA2000 which responds by displaying information relating to status of the peripheral, with a list of the hoppers and their ID-number (except the reject cassette), the number of notes rejected during execution of the command, status of the hoppers (reject cassette included) and, finally, the peripheral firmware release.

TEST 3 - READ CASSETTES ID-NUMBER

Asks the peripheral to give the ID-numbers of the hoppers (reject cassette included), displays them and asks for confirmation. If the operator states that data displayed is incorrect, the numbers are read a second time without any confirmation being given.

TEST 4 - DISPENSE NOTES

A "dispense notes" command is performed. The operator will be required to provide teller number, hopper number and the number of notes to be dispensed. A table is displayed containing the number of the hoppers, their status and the number of notes passed through (rejected notes included).

If the selected teller has notes before the command is given, an error will be reported; then, after 90 seconds (see the CA2000 specifications), a second error is reported as notes are dispensed on a teller not the one selected.

TEST 5 - FORWARD + DELIVERY

This test is comprised of two distinct commands: the "forward" command, which transfers the notes from the feeder area to the stacker and the "delivery" command which transfers the notes from the stacker area to the teller. From the end of the first command to the start of the second, there is an interval of approx. 10 seconds.

A table is displayed containing the number of the hoppers, their status and the number of notes handled (including the notes rejected).

If there are notes on the teller selected before the command is carried out, an error is reported; then, after 90 seconds (see the CA2000 specifications), a second error is reported as notes are dispensed on a teller not the one selected.

TEST 6 - FORWARD + REJECT

This test is comprised of two distinct commands: the "forward" command which transfers the notes from the feeder to the stacker area and the "reject" command which transfers the notes to the reject cassette. Between the end of the first command and the start of the second, there is an interval of approx. 10 seconds.

A table is displayed containing the number of the hoppers, their status and the number of notes handled (including the notes rejected).

TEST 7 - LIFTS DOWN

Peforms the "lifts down" command.

TEST 8 - LIFTS UP

Performs the "lifts up" command.

TEST 9 - READ TRACE

Lists the last 15 error situations.

4.14.2 ERROR AND SERVICE MESSAGES

ERROR MESSAGES

The error messages can be divided in three groups:

1) Blocking errors

- ***** PRIVILEGED INSTRUCTION TRAP *****
- ***** SEGMENT TRAP *****
- ***** NON MASKABLE INTERRUPT *****

If the above errors occur, the system should be switched off or reset.

2) Common interface errors

- **THE PRESENT CONTROLLER IN SLOT XX ANSWERS PHYSICAL NAME YY INSTEAD OF ZZ**
- **THE SLOT XX IS EITHER EMPTY OR CONTAINS A NOT SELFDECLARING CONTROLLER**
- **UNAVAILABLE CA2000 ERROR** : the CA2000 is not connected to the line, is off or is switched off during test execution. In some cases (as in TWIN connection, for example), it indicates that the parameters assigned are different from those set on the CA2000 switches. In an ELB1382 connection, it also indicates that the WS is off and, in this case, if the error is still signalled after the program is run again, the ELB should be reset. This condition is also signalled when DIP-switch 3 of the CA2000 is not correctly set.
- **CA2000 OFF** : the peripheral is off or the connector is not connected.
- **LINE ERROR** : the program parameters do not tally with the values jumpered on the CA2000 DIP-switches. Check the connection between the CA2000 and the system.
- **ELAPSED TIMEOUT – UP NOT READY** : no response from peripheral to system request after a time-out of 30 seconds.
- **INCOHERENT ERROR MESSAGE REPEAT TEST** : fault found is not among scheduled errors.

3) ELB1382/TWIN/UC – CA2000 Errors

- **CHANNEL INITIALIZATION ERROR**
- **NO EXIT NMI DURING RESET FASE** : no reset performed (hardware fault).
- **EMPTY CASSETTE**
- **LIFTS ARE DOWN**
- **WRONG COUNT** : the number of notes counted by the feeder does not match the number counted by the stacker. Fault in feeder or stacker sensor.
- **FAILURE TO FEED**
- **TRANSMISSION ERROR** : the message received by the CA2000 contains an incorrect LRC or parity error. Line parameters incorrect or line operation faulty.
- **ILLEGAL COMMAND**
- **DOUBLE DETECT MALFUNCTION**
- **NOTE CASS. NOT PROPERLY INSTAL.**
- **CLEANING WALL FAILURE**
- **REJECT CASS. NOT PROPERLY INSTAL.**
- **DELIVERY FAILURE**
- **REJECT FAILURE**
- **TOO MANY NOTES REQUESTED** : (more than 100).
- **TOO MANY NOTES ON CONVEYOR**
- **MAIN MOTOR FAILURE**
- **GAIN ON LIMIT**
- **FEEDER SENSOR FAIL**
- **SAME OPERATOR TWICE** : the teller has not picked up the notes made available by the "dispense" or "delivery" commands.
- **COMMUNICATIONS TIME-OUT** : check all cable connections.
- **CASSETTES MAY HAVE BEEN CHANGED** : cassette(s) ID-number not read. First perform test no. 3 "READ CASSETTES ID-NUMBERS".
- **REJECT CASSETTE FULL** : the reject cassette notes counter signals that the number of notes does not yet exceed the limit of 350. The cassette should be emptied as the arrival of more banknotes could result in a LOCK OUT.

- **HOPPER NUMBER STATUS NUM.NOTES**

X	Y	NNNN
X	Y	NNNN
X	Y	NNNN
X	Y	NNNN
X	Y	NNNN
X	Y	NNNN

Message output in tests 4, 5 and 6, where:

X : hopper numbers
Y : hopper status
NNNN : number of notes handled

- ****CONTENTS OF THE REJECT TRACE BUFFER**** : this message is output in test 9 "READ TRACE". The message itself is then followed by a series of messages explaining the last 15 conditions which have resulted in banknotes being rejected.

If, however, there are no significant messages, the following message is displayed:

- **UNUSED POSITION**

4.15 PCA200: CA2000/2020 CONNECTED VIA MUX, ELB3684, WS685/M

PROGRAM PURPOSE

To check operation of the CA2000 (or CA2020) and the physical and logical connection to a MUX, ELB3684 or WS685/M.

HARDWARE REQUIRED

CA2000 or CA2020 unit, MUX board G0322, D-BOX and external hardware loop plug or ELB3684 or WS685/M.

LOOP PLUG

In the case of a D-BOX connection, an external hardware loop plug must be connected to the C.L. or RS 232 line connector of the D-BOX connecting to the CA2000. The following pins must be looped:

2 <---> 3 4 <---> 5 <---> 8 6 <---> 20

WARNING

- The parameters entered by the operator must correspond to those of the CA2000. If they do not, errors will be reported which do not result from CA2000 malfunctions. The CA2000 may be programmed with the 16-position rotary DIP-switch SW3 (DIP-switch SW2 must be kept open).

- If tests 4 and 5 are not carried out in the default sequence, they must be performed after test 3; otherwise, an error is reported.

- If the connection is through ELB3684 or WS685/M, a 30-second timer is set off before all I/O operations so that if nothing of significance occurs, wait until after the time-out for information.

LOADING PROCEDURES

See section 1.3.2.

For other error messages, see section 1.7.3 describing the PCA100 program error messages. Messages referring to the ELB1382 or the TWIN may be ignored.

SERVICE MESSAGES

The following service messages are displayed on the screen of the ELB3684 or the WS685/M:

- **LINE XX** : the message which follows refers to MUX line XX.
- **CHARACTER GENERATOR ROM TYPE : PK3Y/PK3Z**
- **ROM TYPE WS685/M MULTIFUN. CHAR. GEN.**
- **CHARACTER GENERATOR ROM TYPE INCOHERENT**
- **RS232_C LINE A/B CONNECTED/NOT CONNECTED**

For other service messages, see section 1.7.3 with the service messages of the PCA100 program.

5. TEST PROGRAMS FOR SPECIFIC M60 BOARDS

5.1 UCM805: CPU BOARD TEST PROGRAM

PROGRAM PURPOSE

The function of this program is to test the CPU system hardware, in particular the bus arbiter and the watch-dog logic.

HARDWARE REQUIRED

Timing Controller board (TCB), floppy disk controller, video and keyboard controller and hardware loop plug.

NOTE:

The Italian abbreviation UC (Unita Centrale) is sometimes used instead of CPU.

PRESETTINGS

For the serial interface test, a hardware loop plug should be fitted on the CPU board(s), with the pins connected as shown below:

Pin connection:
1 - A 3 - C 5 - E
2 - B 4 - D

LOADING PROCEDURES

Refer to section 1.3.2.

5.1.1 TEST DESCRIPTION

1) SLOT TEST

This test checks that the CPUs (MASTER and SLAVES) are in their correct positions as selected by the operator.

2) MMU SLAVE TESTS

This test checks that the MMU are present and enabled on the slave boards.

3) MEMORY MANAGEMENT UNITS TEST

This test is run when both MMUs are present on the board. The program is subdivided into the following tests:

a) The short circuit test - used to detect any shorts between the bits of the MMU registers and consists of:

b) The address test detects any shorts between the MMU internal address locations.

c) This is a functional test in which a short version of the Abraham-Thatte algorithm is used. The Segment Descriptor Registers are seen as storage divided into bytes.

4) MASTER AND VIENO SIGNALS TEST

Used to verify that the two signals are set and reset correctly.

5) TIMER TEST

The test comprises:

a) Rate generator test (channel 0 in mode 2)

b) Interrupt on terminal count test (channel 1 in mode 0)

c) Square wave rate generator test (channel 2 in mode 3)

6) ACIA (SERIAL INTERFACE) TEST

The ACIA is tested using an internal loop or an external loop on the TxD and RxD signals.

a) Test 1: the 6 service signals (3 input, 3 output) are tested. The loop is made with an external plug (the test is only made if the loop plug is fitted).

b) Test 2 : the ACIA is tested in polling sequence with an external loop of the TxD and RxD signals. Double buffering in receive and send is also tested. If there is no loop plug, the internal loop is used.

c) Test 3: an ACIA test with send interrupt enabled and receive interrupt disabled. The loop plug is required. Test performed with ACIA programmed as follows: clock/16, 8 bits + 2 stop bits. If there is no plug, the internal loop is used.

d) Test 4: an ACIA test with send interrupt disabled, receive interrupt disabled. The loop plug is required. Test is performed with the ACIA programmed as follows: clock/16, 8 bits + 2 stop bits. If there is no plug, the internal loop is used.

e) Test 5: an ACIA test with send and receive interrupts enabled. The loop plug is required. Test is performed with ACIA programmed as follows: clock/16, 8 bits + 2 stop bits. If there is no plug, the internal loop is used.

f) Test 6: a test of the logic of the internal loop on the TxD and RxD signals. The test is only performed if the plug is fitted as the internal loop logic is tested in the subsequent tests.

This test also checks out the ACIA level 2 vectored interrupt, using the first free vector.

7) INTERRUPT TEST

a) Non-vectored interrupts:

The test comprises:

- a test of the input port on which the reason for the interrupt and the mask status are read. Certain values are input to the latch, interrupt signals and masks are set and reset, with all interrupts disabled and the contents are then read and compared.
- a test of the interrupt generated by signal NV1
- a test of the interrupt generated by signal NV2
- a test of the interrupt generated by signal NV3
- a test of the interrupt generated by signal NV4
- a test of the interrupt generated with several interrupt signals set.

In the NV2, NV3 and NV4 signal tests, the mask signals are also tested to be effective.

b) Vectored interrupt:

In this test, a vectored interrupt is generated with the following interrupt vectors:

0,2,4,8,10,20,40,80,Ce',E0,F0,F8,FC,FE

Section 1 of the timer and the ACIA are used to generate the interrupt. Besides testing the interrupt logic, this test is also designed to test the registers designated to hold the timer and ACIA interrupt vectors.

- Non-maskable software interrupt:

  In this test, a non-maskable software interrupt is generated; a check is then made that the interrupt has occurred.

- Non-maskable interrupt for TCB alarm:

  This test checks that the interrupt has occurred after simulating 15 single errors and 1 double error. The test also checks that the NMIBC signal is correctly stored in the appropriate latch.

- Non-maskable interrupt (IPC) for implementation of interprocessor communication in a multi-processor environment:

  The interrupt is generated and checked to have occurred. The test also checks that the IPC signal is correctly stored in the appropriate latch.

8) ABORT TEST

In this test, all instances in which an abort is generated are simulated and a check made that: the trap is generated, the MMU Status Registers and the hardware register store the correct data.

The memory disable flip-flop is also tested.

9) ROM TEST

The ROM bank test is made by comparing the CRC with the contents of the last 4 bytes of the ROM.

10) EAROM TEST

a) The short circuit test reveals any shorts between bits of a cell.

b) The address test reveals shorts between locations with different addresses.

c) A shortened version of the Abraham-Thatte test is used for a functional check.

11) SWITCH TEST

The status of DIP-switches on the board is read and compared with the value entered by the operator. If the values differ the switch status is displayed.

12) WATCH-DOG TEST

This test checks that all main memory changes made by CPU's are consistent and are reflected on the Cache memories of the other CPU's. This is done to check that all CPU's present in the system have access to the same data. If the Cache is not present the test is not carried out.

13) BUS ARBITER

This test consists of running a program on all the CPU's in the system, causing several bus requests to be made at the same time; the test then checks that the correct bus priority is established.
The test continues with the Cache enabled and then disabled.

14) RESET TEST

This is a controlled test in which the hardware of peripherals connected is reset. The CPU is not reset. The system should be reset after the test.

5.1.2 ERROR AND SERVICE MESSAGES

The majority of the following error messages refer to the CPU, therefore change this board first, if this fails clear the error try changing the TCB.

Test 1 message:

- **INCORRECT UC MASTER SLOT NUMBER**

Test 2 messages:

- **SLAVE #1 NOT READY**
- **SLAVE #2 NOT READY**

Test 3 messages:

- **SHORT ERROR ON THE MR (MMU2/MMU1)**
- **SHORT ERROR ON THE SAR (MMU2/MMU1)**
- **SHORT ERROR ON THE DSCR (MMU2/MMU1)**
- **SHORT ERROR ON THE SDR (MMU2/MMU1)**
- **SDR ADDRESS FAULT (MMU2/MMU1)**
- **DYNAMIC TEST FAULT (MMU2)**
- **FUNCTIONAL ERROR (MMU1)**

Test 4 messages:

- MASTER SIGNAL STUCK AT 0/1
- VIENO SIGNAL STUCK AT 0/1

Test 5 messages:

- COUNTER 0/2 FAULT
- COUNTER 1 INTERRUPT FAULTING
- LATCH OUTPUT CNT1 FAULT

Test 6 messages:

- SIGNAL POx STUCK AT 1/0 OR LATCH FAULT
- SIGNAL PO1/PO2/PO3 OR LATCH FAULT
- TIME-OUT ERROR ON TX/RX READY
- DOUBLE BUFFERING FAULT
- ERROR FLAGS STUCK AT 0/1
- FRAMING ERROR
- OVERRUN ERROR
- PARITY ERROR
- WRONG DATA RECEIVED
- TIME-OUT ERROR ON LAST TX DATA
- UNKNOWN INTERRUPT

Test 7 messages:

- NVx & ENx: WROTE 1/0 READ 0/1
- INTERRUPT NV1/NV2/NV3/NV4 FAULT
- NV1/NV2/NV3/NV4 INTERRUPT MASK FAULT
- CONCURRENT INTERRUPT FAULT
- NO TIMER INTERRUPT
- BAD VECTOR TIMER INTERRUPT
- BAD VECTOR ACIA INTERRUPT
- NO IPC INTERRUPT

- IPC SIGNAL OR LATCH FAULT
- NMI SOFTWARE NOT OCCURRED
- NO ALARM TCB INTERRUPT (WARMA)
- NO ALARM TCB INTERRUPT (NOMIN)
- LATCH NMI FAULT

Test 8 messages:

- VIOL.TYPE REG. FLAGS FAULT
- RDV TRAP NOT OCCURRED
- VIOL. TYPE REG. FAULT
- VIOL.SEG.NUM.REG.FAULT
- VIOL. OFF.REG. FAULT
- BUS CYCLE STATUS REG. FAULT
- INST.SEG.NUM.REG.FAULT
- INST.OFF.REG FAULT
- HW REGISTER FAULT
- XXXX TRAP NOT OCCURRED
- XXXX TRAP OCCURRED
- FATAL CONDITION FAULT
- FATAL FLAG STUCK AT 0
- DISABLE INHIBITION MEMORY FAULT
- ENABLE INHIBITION MEMORY FAULT

Test 9 messages:

- LOW BANK FAULT
- HIGH BANK FAULT
- BANK FAULT

Test 10 messages:

- SHORT DATA ERROR ON EAROM
- SHORT ADDRESS ERROR ON EAROM
- EAROM NOT TYPE 64 X 4

Test 11 messages:

- SWITCH ON BOARD UC SLOT - X
  READ IN0 = X EXPECTED X
  READ IN1 = X EXPECTED X
  READ IN2 = X EXPECTED X
  READ IN3 = X EXPECTED X

Test 12 messages:

- WATCH DOG ERROR
- NO CACHE

Test 13 messages

- MODE PARAMETER ERROR
- TARGET CPU NOT PRESENT
- TARGET NAME SAME AS SOURCE NAME
- TARGET CPU NOT READY
- TARGET CPU DOES NOT ACKNOWLEDGE

Other messages:

- MASTER : TEST ERROR
- SLAVE #1 : TEST ERROR
- SLAVE #2 : TEST ERROR

5.2 CACH84: CACHE BOARD TEST PROGRAM

PROGRAM PURPOSE

The program is designed to check that all parts of the CACHE board are functioning correctly.

HARDWARE REQUIRED

CU board, memory board, CACHE board.

LOADING PROCEDURES

Refer to section 1.3.2.

5.2.1 TEST DESCRIPTION

1) CACHE I/O TEST

DATA TEST.

Checks that there is no short circuiting or coupling between the 16 data bits on any memory address, using incremental addressing.

ADDRESS TEST.

Same as previous test, except that address bits are tested.

FUNCTIONAL TEST.

Based on the algorithm for the cache memory test with the complete error model, as proposed by R. Nair, S.M. Thatte and J.A. Abraham. Using incremental addressing, the windows defined by the addresses and input size are read and checked that they contain the background pattern; then the test pattern is written and a further check made.

SHORT FUNCTIONAL TEST.

This is a short version of the Nair, Thatte and Abraham test. Though less comprehensive, execution time is greatly reduced.

2) ASSOCIATIVE I/O TEST

DATA TEST AND ADDRESS TEST.

These two tests are similar to the cache I/O tests but apply to the associative memory.

COMPARATOR TEST.

The comparators are tested by inputting first a number of identical patterns and checking that the output is 0, then a number of odd patterns and checking that the output is 1.

3) CACHE/ASSOCIATIVE MEMORY TEST

WRITE THROUGH TEST

This test enables the cache memory and writes into a memory space in the cache.

The cache memory is then disabled and the data checked to see if it has been correctly written into the main memory.

DATA TEST, ADDRESS TEST AND FUNCTIONAL TEST.

These three tests are the same as the previous tests on cache memory; the cache is however enabled and disabled to check that the memory has been written to correctly.

4) LOGIC TEST

BURST TEST.

This tests BLOCK reading in memory in the event of a MISS.

DOUBLE BURST TEST

This tests verifies the correct transfer in double burst.

WATCH DOG TEST.

This test is performed at the request of the operator as it can only be run on the correct hard disk unit.

The test checks for the presence of the hard disk, reads a special track and checks that the cache memory is disabled.

5.2.2 MESSAGES OUTPUT

** PRIVILEGED INSTRUCTION TRAP **

- ** SEGMENT TRAP **
- ** NON MASKABLE INTERRUPT **
- I/O ADD XXXX READ YYYY EXPECTED ZZZZ
- ADD: XXXXXX READ YYYYYY EXPECTED ZZZZZZ
- ADD: XXXXXX NO MEMORY READY
- FUNCTIONAL TEST RUNNING
- SHORT FUNCTIONAL TEST RUNNING

- CACHE BOARD OR CPU LOOP ABSENT
- P.U. FAILURE
- VERIFY PARAMETERS
- DATA ERROR
- UNRECOVERABLE ERROR
- WATCH DOG ERROR

NOTE:

1) After receiving one of the following messages the system must be reset:

```
** PRIVILEGED INSTRUCTION TRAP **
** SEGMENT TRAP **
** NON MASKABLE INTERRUPT **
```

2) The messages shown below are displayed if memory (cache and/or associative) read errors occur:

```
I/O ADD XXXX READ YYYY EXPECTED ZZZZ
ADD: XXXXXX READ YYYYYY EXPECTED ZZZZZZ
where:
X = the address at which the error occurred
Y = data read
Z = data expected.
```

3) The following message is displayed as a result of a memory overflow at address XXXXXX:

```
ADD: XXXXXX NO MEMORY READY
```

4) The following messages are service messages only, indicating that the tests are running:

```
FUNCTIONAL TEST RUNNING
SHORT FUNCTIONAL TEST RUNNING
```

5) The following message is displayed if PLUG or CACHE BOARD is missing:

```
CACHE BOARD OR CPU LOOP ABSENT
```

6) The remaining messages are associated with the disk unit.

5.3 TCB805: TCB TEST PROGRAM

PROGRAM PURPOSE

The function of the program is to test the Timing Control Board (TCB).

HARDWARE REQUIRED

Timing Control Board

LOADING PROCEDURES

Refer to section 1.3.2.

5.3.1 TEST DESCRIPTION

STATUS AND ORDER REGISTER TEST

The test consists of reading the status register and testing the DECCO signal. If the DECCO signal is at level 1, the test is exited because there is a blocking error (at level 0, the ECC functions are enabled).

The status register is read and tested to see if the register is clear. If the register is not clear i.e. any bits at 1, the test is exited because there is a blocking error. If the program is run in loop mode, the above is significant only during the first cycle (after a reset).

In the order register the bits are set to 1 sequentially. At each change the status register is read and tested to ensure the changes correspond.

ERROR LOGGING MEMORY TEST

0's are written in all memory cells; the cells are then read and checked to see if there are any bits stuck at 1. 1's are written in all memory cells; the cells are then read and checked to see if there are any bits stuck at 0. 1's are written in the first cell and 0's in the remaining cells. The cells with the complementary addresses are then read incrementally. Address bits stuck at 0 are detected. 0's are written in the last cell and 1's in the remaining cells. The cells with the complementary addresses are then read decrementally. Address bits stuck at 1 are detected.

The shortened version of the Abraham test is run on memory.

ECC TEST

This test checks for shorts between the bits in the status register used for the control code or syndrome pattern. The test verifies that the ECC calculates, during the write cycle, the control pattern correctly. Then checks, during the read cycle, that the control pattern in memory is stored in the status register and signals SERRO and MERRO remain at 0.

32 single bit errors are then produced, and tests made to see if the ECC has correctly calculated the syndrone pattern. The test also checks that the ECC sends out the corrected data on the bus when an error is encountered.

SINGLE ERROR TEST

15 errors are generated by modifying a single bit in 15 different memory cells. At each memory read a check is made to see if signal SERRO is at 1 and that the correct data is sent on the bus. After 15 reads, signal OWRFN should go to 1 (this checks the single bit error counter) and data in the error logging memory should be updated.

MULTIPLE ERROR TEST

This test checks that when a double error is generated, during a read oneration, signal MERRO goes to 1.

INTERRUPT TEST

This test checks that an interrupt is generated after the ECC has found 15 single errors or a double error.

ARRAY REFRESH TEST

Checks that spurious errors are cleared when memory is refreshed.

BURST TEST

This test checks that, when the bus master initiates the BURST protocol by addressing the first DWORD, the next 3 DWORDs are addressed by the TCB by sending the address bits ADA2C and ADA3O in loop mode. The test is run only if the operator has selected the CACHE ENABLE option.

5.3.2 ERROR MESSAGES

The majoroity of the errors listed below refer to the TCB, therefore if an error occurs change this board first.

- ECC ERROR RETRY
- TCB STATUS ERROR
- AELOO/ERROR LOGGING STUCK AT 0
- ABNOO/NOMINAL STUCK AT 0
- ESERO/REFRESH CORR. STUCK AT 0
- AELOO/ERROR LOGGING STUCK AT 1
- AENOO/NOMIN STUCK AT 1

- ESERO/REFRESH CORR. STUCK AT 1
- DECCO/ECC STUCK AT 0
- DECCO/ECC STUCK AT 1
- ERR.LOG OR BIT 15 STATUS REG. FAULT
- ADDRESSS ERR. LOG STUCK AT 0
- ADDRESS ERR. LOG STUCK AT 1
- DYNAMIC TEST FAULT
- CB ON WRITING FAULT
- CB ON READING FAULT
- SERRO STUCK AT 1
- MERRO STUCK AT 1
- ECC DOES NOT CORRECT SINGLE ERROR FAULT
- SYNDRONE PATTERN FAULT
- SERRO STUCK AT 0
- MERRO STUCK AT 0
- OWRFN STUCK AT 0
- ERROR LOGGING MEMORY NOT UPDATED
- MERRO STUCK AT 0
- TCB INTERRUPT NOT OCCURRED (OVERFLOW)
- TCB INTERRUPT NOT OCCURRED (DUPLEX ERR).
- SCRUBBING NOT EFFECTED
- BURST TRANSFER ERROR

5.4 MEM813: RAM TEST PROGRAM

PROGRAM PURPOSE

To check that the system RAM functions correctly.

HARDWARE REQUIRED

M60 system RAM boards (RA800, RA800/A, RA80/A-D, RA80/F, RA80/H, RA80/N).

LOADING PROCEDURES

Refer to section 1.3.2

GENERAL/PRELIMINARY INSTRUCTIONS

Refer to section 3.8 of the MEM812 program

5.4.1 TEST DESCRIPTION

Refer to section 3.8.1.

5.4.2 ERROR MESSAGES

Refer to section 3.8.2

Also note the addition of the following messages:

- * X * at add. 00yyyyyy multiple error = during execution of test X, at address yyyyyy a parity bit error signal has been received.

- * X * at add. 00yyyyyy overflow error = during execution of test X, at address yyyyyy a parity bit error signal has been received.

5.4.3 OTHER MESSAGES

The following messages can be displayed in addition to those shown in section 3.8.3.

*** WARNING CACHE ENABLED ***

*** WARNING ECC ENABLED ***

*** WARNING TCB ALARM ENABLED ***

*** WARNING ERROR OVERFLOW DISABLED ***

These messages indicate that the tests are not complete.

5.4.4 LOCATION OF FAULTY RAM CHIP

The location of the faulty RAM chip is determined using the following tables as indicated:

Example:

ERROR MESSAGE:

Mbyte 1 bank 2 syndrome 6C

1) Using the syndrome number (6C) refer to table (a) to obtain the faulty DATA/CONTROL bit (in this case D 18).

2) If the RAM chip is 64Kb (i.e. boards RA80D, RA80D, RA800A, RA80F), then using the bank value (B2) and the CONTROL/DATA bit (D18) as co-ordinates determine the location of the faulty chip by referring to diagram (a).

3) If the RAM chip is 256Kb (i.e. boards RA80N, RA80C, RA80B, RA80A, RA80H) then using the Mbyte value (M1) and the CONTROL/DATA bit (D18) as co-ordinates determine the location of the faulty chip by referring to diagram (b).

SYNDROME NUMBER	DATA BIT (ERROR)	SYNDROME NUMBER	DATA BIT (ERROR)
30	D0	66	D21
35	D1	65	D22
2D	D2	63	D23
2B	D3	1D	D24
28	D4	1B	D25
27	D5	18	D26
24	D6	17	D27
22	D7	14	D28
5C	D8	12	D29
5A	D9	0F	D30
59	D10	0A	D31
56	D11		
55	D12		CONTROL BIT
53	D13		(ERROR)
4E	D14	7E	C0
4B	D15	7D	C1
71	D16	7B	C2
74	D17	77	C3
6C <--	D18	6F	C4
6A	D19	5F	C5
69	D20	3F	C6

--- SYNDROME NUMBER

TABLE (a) SYNDROME NUMBER-DATA/CONTROL ERROR BIT

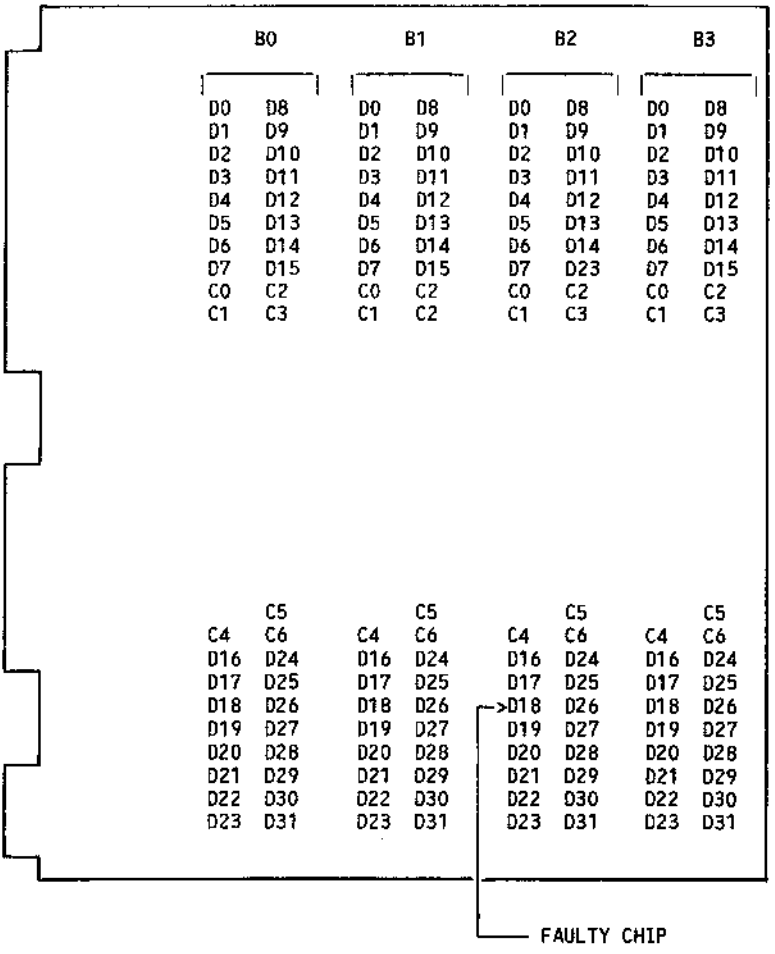


DIAGRAM (a)- COMPONENT LOCATION DIAGRAM FOR BOARDS CONTAINING 64Kb CHIPS (VIEW ON COMPONENT SIDE)

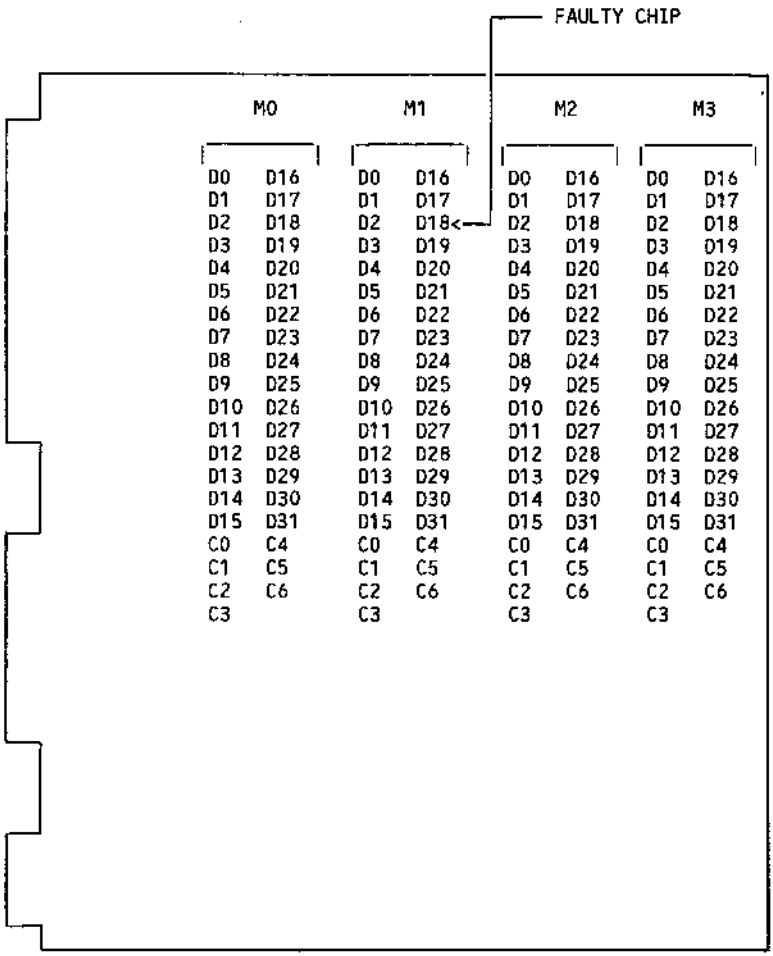


DIAGRAM (b)- COMPONENT LOCATION DIAGRAM FOR BOARDS CONTAINING 256Kb CHIPS (VIEW ON COMPONENT SIDE)

5.5 MREDA3: REDAC BOARD TEST PROGRAM

PROGRAM PURPOSE

This program is designed to check that the CPU/REDAC, REDAC/CONSOLE and REDAC/UC SLAVE communication ports function correctly.

HARDWARE REQUIRED

Central unit board, memory board, TCB, floppy disk controller, video and keyboard controller, CACHE and REDAC board.

LOADING PROCEDURES

Refer to section 1.3.2.

5.5.1 DESCRIPTION OF PROGRAM

In the REDAC test program, a number of console functional checks are run. The operator's role is to check that the console parts tested respond correctly. If an automatic switch-off, followed by automatic switch-on is programmed, the operator must set the key to stand-by; otherwise, the operation is ignored.

5.5.2 ERROR MESSAGES

For error messages occurring in test execution, see table below:

TYPE OF ERROR	CAUSE	ACTION
Timer 8253 no go	Counter 8253 is not working	Replace REDAC board timer in position D06
Z80CTC no go	Z80 CTC not working	Replace Z80 (Position F06)
Z80 SIO no go	Z80 SIO not working	Replace Z80 SIO (position B06)
line loop no go	Line loop not working	Replace NED4C board
FEC interface (teled.Key)no go	FEC interface (telediagnostic key) not working	Replace NED4C board

TYPE OF ERROR	CAUSE	ACTION
RAM OL (E000-E3FF) no go	RAM not working	Replace RAM 0 in position E 10
RAM OH (E400-E7FF) no go	RAM not working	Replace RAM 1 in position D08
ROM OL (0000-0FFF) RAMOH (1000-3FFF) no go	ROM 0 not working	Replace ROM 0 in position A10$
ROM 1 (4000-7FFF) no go	ROM 1 not working	Replace ROM 1 in position B 10
ROM 2 (8000-BFFF) no go	ROM 2 not working	Replace ROM 2 in position C 10
Real time clock no go	Clock not working	Replace REDAC board
PARAMETER MODE ERROR	-	-
TARGET CPU NOT PRESENT	-	-
TARGET NAME SAME AS SOURCE NAME	-	-
TARGET CPU NOT READY	-	-
TARGET CPU DOES NOT ACKNOWLEDGE	-	-
SLAVE1 NOT READY	-	-
SLAVE2 NOT READY	-	

5.6 CAC603: CACHE BOARD TEST PROGRAM (ON 60Mb FUJITSU)

PROGRAM PURPOSE

The program is designed to check that the CACHE boards function correctly.

HARDWARE REQUIRED

CACHE 8000 board and CACHE-CPU connection.

LOADING PROCEDURE

Refer to section 1.3.2.

5.6.1 TEST DESCRIPTION

The test performed on each CACHE board, whether MASTER or SLAVE, is as described in the CACH84 program, section 5.2.1.

5.6.2 ERROR MESSAGES

The error messages are the same as listed in the CACH84 program, section 5.2.2, with the addition of the following messages:

- INCORRECT UC MASTER SLOT NUMBER
  displayed if the MASTER controller board is in the wrong slot,

- SLAVE 1/2 NOT READY
  displayed if a SLAVE controller board has not been initialized.

5.7 CAC123: CACHE BOARD TEST PROGRAM (ON 120Mb FUJITSU)

PROGRAM PURPOSE

The program is designed to check that the CACHE boards function correctly.

HARDWARE REQUIRED

CACHE 8000 board and CACHE-CPU connection.

LOADING PROCEDURE

Refer to section 1.3.2.

5.7.1 TEST DESCRIPTION

The test performed on each CACHE board, whether MASTER or SLAVE, is as described in the CACH84 program, section 5.2.1.

5.7.2 ERROR MESSAGES

The error messages are the same as listed in the CACH84 program, section 5.2.2, with the addition of the following messages:

- INCORRECT UC MASTER SLOT NUMBER
  displayed if the MASTER controller board is in the wrong slot,

- SLAVE 1/2 NOT READY
  displayed if a SLAVE controller board has not been initialized.

6. VIDEO/KEYBOARD TEST PROGRAM

6.1 RAMVID: VIDEO RAM TEST PROGRAM

PROGRAM PURPOSE

To check the operation of the video controller RAM, by writing a character sequence into the RAM and then displaying the corresponding test pattern.

HARDWARE REQUIRED

Video-keyboard controller.

LOADING PROCEDURES

Refer to section 1.3.2

6.1.1 PROGRAM DESCRIPTION

Displays the start and end addresses of the section of RAM under test.

Writes a string of characters into RAM which, after a RAM read, cause a square grid to be generated across the screen with a flashing segment in each square. The grid remains on the screen for 4 seconds, then disappears while the RAM contents are erased. The string is then re-written into the RAM and again the grid displayed but this time for only 2 seconds.

6.1.2 ERROR MESSAGES

If there are errors the following messages are displayed indicating the chip containing the error and bank number (also indicated for 2nd level diagnostics: address, ref. no and test no.):

- CHANGE CHIP RAM XXXX BANK XX — For 1st level diagnostic messages

- CHANGE CHIP RAM XXXX BANK XX
  ADDRESS XXXXXX REF XXXX
  TEST XXXX — For 2nd level diagnostic messages

6.2 CRTAN5 :TRIVALENT ALPHANUMERIC VIDEO TEST PROGRAM

PROGRAM PURPOSE

To check the operation of the video by displaying all the attributes on the screen.

HARDWARE REQUIRED

Video-keyboard controller, video.

LOADING PROCEDURES

Refer to section 1.3.2

PROGRAM DESCRIPTION

Initially the program displays the main features of the video e.g. type, number of rows, total number of characters and row length. Then the following tests are carried out:

TEST 1

A sequence of characters (ABC...) read from ROM is displayed on the video.

TEST 2

The screen is filled progressively with "H" characters starting from the bottom of the screen; if the 9 inch video is used the process is repeated with "M" characters.

TEST 3

The screen is filled progressively with "O" characters starting from the top left hand corner of the screen.

TEST 4

The screen is filled with "O" characters. Each character is displayed with one of the following attributes as indicated on the first line of the display:

- high graphic line
- low graphic line
- left graphic line
- right graphic line
- blinking (BL)
- high light (HL)
- reverse video (RV)
- graphic line + blinking
- graphic line + high light
- graphic line + reverse video

6.2.1 ERROR MESSAGES

If the wrong video controller is selected, the message UNIT NOT PRESENT is displayed and the selection string repeated. If an incorrect entry is made during tests the following message is displayed: CRT BAD WORKING - otherwise (if there is an error) the standard MONITOR error mask is displayed.

6.3 CRTGR2: GRAPHIC VIDEO TEST PROGRAM

PROGRAM PURPOSE

To ensure that the graphic video and its controller are functioning correctly.

HARDWARE REQUIRED

Video-keyboard controller, graphic video controller, graphic video.

LOADING PROCEDURES

Refer to section 1.3.2

6.3.1 PROGRAM DESCRIPTION

TEST 1 : FIXED PATTERN

A fixed test pattern is written, the data written is then read and compared with the original data used in writing. This procedure is repeated 24 times, with a new test pattern each time.

TEST 2 : ADDRESS

Each memory location has its address written into it, after which memory is checked to verify correct addressing. Byte addressing is used so that odd and even addresses can be checked.

The process is repeated using the 2's complement of the addresses written earlier.

TEST 3 : MARCHING

The first 12 sequences of the FIXED PATTERN test are used again. The first sequence is written, read and checked; then its complement, and the remaining sequences and their complements are written, read and checked. The entire cycle is then repeated.

TEST 4 : BUSS NOISE

A sequence is written into memory, using the Z 8001 instruction (ldir). A check is then made using the instruction (cdir).

The cycle is repeated with 24 fixed patterns.

TEST 5 : REFRESH

The whole of memory is written with the sequence AA55. After a delay of 1 second the data is read and compared with the original data.

6.3.2 ERROR AND SERVICE MESSAGES

If there is an error in controller selection, the following message is displayed:

MISSING CONTROLLER

If there is an error as a result of tests 1 to 4, the following message is displayed:

ADDRESS XX XXXX WRITTEN XXXX READ XXXX

6.4 KEYTE1: KEYBOARD TEST PROGRAM

PROGRAM PURPOSE

To check the correspondance between characters output from the keyboard microprocessor and characters requested and also to check the operation of the LED indicators.

HARDWARE REQUIRED

Video-keyboard controller, keyboard.

GENERAL

- **ALPHANUMERICAL KEYBOARD**

  The keys are operated in sequence from left to right, starting from row 1 (top row) and ending on row 5 (bottom row). All keys, including the SHIFT, LOCK and CONTROL keys, must be tested. The double key, common to both row 3 and row 4, must be operated ONLY when testing keys on row 4.

- **FUNCTION/NUMERICAL KEYBOARD**

  The keys are tested in the same way as in the ALPHANUMERICAL KEYBOARD tests except that the double keys (not 0) are operated each time a row (common to the double key) is tested.

LOADING PROCEDURES

Refer to section 1.3.2

6.4.1 TEST DESCRIPTION

Initially the status of the keyboard jumpers are displayed together with the release date. The keyboard name can then be obtained by reading the jumper status and referring to the table of names. The program then displays a selection of KEYBOARD LAYOUTs and proceeds with the following tests (after a selection is made):

NOTE

In the case of the 80 character/line VDU a table is displayed showing the character sets of the ROM VDU controller and keyboard which should correspond.

TEST 1 - ALPHANUMERICAL KEYS

This test checks the operation of the key switches and the alphanumerical keys:

a) The key switches are tested by turning key(s) to the right and verifying that the video displays "RIGHT", then turning the key(s) to the original position(s) and verifying that the video displays "NORMAL".

b) The alphanumerical keys are tested by operating the keys indicated on the display and verifying that the keys hit correspond to the codes displayed under the keyboard plan.

N.B. The keys to be hit are indicated by a blinking code on the plan.

TEST 2 - FUNCTION/NUMERICAL KEYS

The function/numerical keys are tested as in test 1

TEST 3 - LEDS/SPECIAL KEYS

The LEDS are checked by observing that they go on and off in the following order:

1. READY LED,
2. L1 LED,
3. L2 LED
4. SHIFT LED.

Special keys are tested by operating the keys at least four times and verifying that the codes displayed correspond and in particular the following:

1. When LK is pressed code 6F is displayed and when released code 77 is displayed.
2. When SH is pressed code 6E is displayed and when released code 76 is displayed.
3. When CN is pressed code 70 is displayed and when released code 78 is displayed.
4. When 2 keys are pressed simultaneously code FE is displayed.

To exit the test the following keys of the funtion/numerical keyboard must be hit:

1. First top left key (44 on the display)
2. Last top right key (39 on the display)
3. Last bottom right key (3F on the dispaly)

TEST 4 - SHIFT KEYS

The operation of the SHIFT key is tested by hitting all the alphanumerical keys in turn initially to display small letters and then capitals (using the SHIFT key).

The RESET key should then be operated and checked followed by the operation of the key immediately above the SKIP bar in order to exit tests.

6.4.2 ERROR MESSAGES

If an incorrect key is hit in TEST 1 or TEST 2, the video displays:

- RECEIVED: XX - HIT ENTER TO RETRY -

where XX is the code of the key hit.

To continue: Hit ENTER and then SKIP to test remaining keys.

6.5 GRAPH3: COLOUR VIDEO CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To test the colour graphic/alphanumeric video controller.

HARDWARE REQUIRED

Colour graphic and/or alphanumeric video controller (GO259/260/261).

PRELIMINARY OPERATIONS

If the RS232 serial interface lines are to be tested fit plugs on the serial I/O connectors of the graphic/alphanumeric controllers with the following connections made:

On alphanumeric controller	On graphic controller
Pin 8 linked to Pin 1 Pin 9 linked to Pin 9 Pin R linked to Pin S	Pin 13 linked to Pin 14

LOADING PROCEDURES

Refer to section 1.3.2

6.5.1 TEST DESCRIPTION

1) TOTAL/PARTIAL ALPHA MEMORY TEST

The part of the memory used for storing characters and attributes are checked using the following tests:

- **CURSOR 7220 TEST**

  The test checks that there are no shorts between the bits of the 7220 cursor and that the cursor is automatically incremented in read and write from high to low and from low to high.

- **DATA SHORT TEST**

  The test uses the %55 and %AA patterns to check for shorts between bits and coupling between contiguous cells.

- **ADDRESS SHORT TEST**

  The test checks that there are no shorts between the address bits.

- **FUNCTIONAL TEST**

  The test uses the Abraham-Thatte algorithm to check for dynamic errors under critical conditions. The reduced version of this test, if selected in the pre-program, will reduce execution time but will be less comprehensive than the full version.

  Pattern used is:

  %00 %01 %03 %07 %0F %1F %3F %7F %FF

- **MEMORY CYCLE TEST**

  The test checks the memory write modes.

2) ALPHA LUT (LOOKUP TABLE), THE COUNTER ADDRESS LUT AND MEMORY TEST

These areas and associated buffers are tested using DATA SHORT TEST, ADDRESS SHORT TEST and FUNCTIONAL TEST as already described in the ALPHA MEMORY TEST except that the pattern used is: %0 %1 % %7 %F.

3) ALPHA I/O TEST

The ACIA which controls the serial communication channel with the keyboard is checked as follows (provided that the LOOP PLUG is in place and indicated in the pre-program):

- runs a polling sequence test using the external loop for the TxD and RxD signals.
- runs a transmission test using the external loop with the TX/RX interrupt status as follows:
  - TX enabled and Rx disabled,
  - TX disabled and RX enabled,
  - TX and RX both enabled,

4) ALPHA INTERRUPT TEST

The test checks the keyboard and the following VERTICAL FIELD interrupts:

0,2,4,8,10,20,40,80,C0,E0,F0,F8,FC,FE

5) TOTAL/PARTIAL GRAPHICS MEMORY TEST

The test checks the three graphic memory layers are the same as in the ALPHA MEMORY TEST except that the pattern used is: %A55A.

6) OLIBUS LOOKUP TABLE

The OLIBUS LUT and associated components are tested as in the ALPHA LUT TEST except that the test pattern used is:

%0000 %0FC0 %0A95

7) OLIBUS I/O TEST

The ACIA controlling the Joystick is checked as in the ALPHA I/O TEST.

8) GRAPHICS INTERRUPT TEST

The test checks the JOYSTICK and VERTICAL FIELD interrupts as in the ALPHA INTERRUPT TEST.

6.5.2 ERROR AND SERVICE MESSAGES

- **SHORT DATA ERROR ON CHARACTER (ATTRIBUTE) MEM.**: indicates short circuit between data bits in memory area reserved for attribute characters.
- **SHORT ADD. ERROR ON CHARACTER (ATTRIBUTE) MEM.**: indicates short circuit between data bits in memory area reserved for the attribute character addresses.
- **FUNCTIONAL ERROR ON CHARACTER (ATTRIBUTE) MEM.**
- **LOAD OR ENABLE ERROR ON CNTX** (CNTX = counter X)
- **SHORT ERROR ON CNTX**
- **COUNT ERROR ON CNTX**
- **COUNT CNTX OR CNTY ERROR**
- **ENABLE LUT ERROR**
- **SHORT DATA ERROR ON LUT** : short circuit on data in LUT
- **SHORT ADDRESS ERROR ON LUT**
- **FUNCTIONAL ERROR ON LUT**
- **TIME-OUT ERROR ON TX (RX) READY**
- **DOUBLE BUFFERING FAULT**
- **WRONG DATA RECEIVED**

- **NO KEYBOARD INTERRUPT**
- **NO VERTICAL FIELD INTERRUPT**
- **BAD VECTOR KEYBOARD INTERRUPT** : (incorrect keyboard interrupt vector)
- **BAD VECTOR VERT. FIELD INTERRUPT**
- **UNKNOWN INTERRUPT**
- **NO JOYSTICK INTERRUPT**
- **BAD VECTOR JOYSTICK INTERRUPT**
- **SHORT DATA ERROR PLANE X** : short circuit on data in graphic memory layer X
- **SHORT ADDRESS ERROR PLANE X:** short circuit on addresses in graphic memory layer X
- **FUNCTIONAL ERROR PLANE X**
- **ERROR SELECTION PLANE X**
- **DISABLE VERTICAL FIELD INTERRUPT FAULT**
- **INTERNAL CURSOR 7220 ALPHA (GRAPH) FAULT**
- **READ MODIFY WRITE CYCLE ERROR**
- **TIME-OUT (draw. in prog. stuck at 1)**
- **TIME-OUT (fifo full stuck at 1)**
- **TIME-OUT (data ready stuck at 0)**
- **TIME-OUT (vert sync stuck at 0 (1))**

6.6 T31103: GRAPHIC COLOUR VIDEO TEST PROGRAM

PROGRAM PURPOSE

To test and permit regulation of the graphic colour video.

HARDWARE REQUIRED

Graphic and alphanmumeric colour video controller (G0259/260/261), graphic colour video and standard video, keyboard and controller.

GENERAL

This test program describes the procedure used to regulate the graphic colour monitor picture and regulation of colour intensity.
To perform the regulations, see CTF ("Capitolato Tecnico di Fornitura") No. 110599V01 for readings, tolerances and calibrations.

LOADING PROCEDURES

Refer to section 1.3.2

6.6.1 TEST DESCRIPTION

The program, by using a number of tests, permits the graphic monitor to be set correctly and the colour tone to be regulated.

The tests are:

- MISCONVERGENCE
- GEOMETRY
- LINEARITY
- DISTORTIONS
- DYNAMIC
- PHOTOMETRIC
- COLOURS
- SPOT SIZE
- COLOURS TYPE
- PATTERN

The tests can be individually selected or selected in sequence.

Individual test procedures for measurements and adjustments are displayed on the colour video when HELP is accessed during a test. Reference should be made to the CTF documentation for specific test data.

A brief description on individual test procedures are given in the following section.

N.B.

There are no service/error messages for these tests other than the MONITOR messages (slot no. details etc) and the HARDWARE OK/FAULT message.

6.6.2 INDIVIDUAL TEST PROCEDURES

1. **MISCONVERGENCE TEST.**

   Take the horizontal and vertical misconvergence readings using the appropriate equipment (such as an RCA PIX 503G).

   Check that the readings comply with the standards of the CTF ("Capitolo Tecnico di Fornitura" = Chapter on Supplied Goods Technical Specifications).

   If not, inform the AQL (Quality Assurance division).

2. **GEOMETRY TEST.**

   Using an appropriate mask (or a transparent, flexible ruler) check the screen dimensions conform to the CTF recommendations. CTF.

   If not, the following can be adjusted:

   - Trimmer VR402 for vertical adjustments
   - Winding L505 for horizontal adjustments

   Any pincushion or barrel distortion should be eliminated by adjusting potentiometer VR404.

   To centre the picture horizontally, use first PHASE potentiometer VR707 H, then, if necessary, potentiometer VR502.

   To centre vertically, use potentiometer VR403.

3. **LINEARITY TEST.**

   Use the ruler or mask to take the linearity readings and check that they comply with the CTF recommendations.

4. **DISTORTION TEST.**

   Sight check for dynamic distortion; if there is evidence of distortion the monitor must be repaired.

5. **DINAMIK TEST.**

   Use a mask to check that distortion on the left or right sides of the monitor is within the permitted CTF limits.

6. **PHOTOMETRIC TEST.**

   With a photometer, take a number of white luminosity readings and check they come within the CTF limits.

   If the luminosity does not comply, then the procedure described in the Service Manual code no. 3963450 B should be implemented.

7. **COLOUR TEST (FOR IN-HOUSE USE ONLY).**

   A white square drawn on the centre of the screen is used to check and regulate white luminosity as described in the STAC manual.

   The other colours may also be checked (proceed as per menu).

8. **SPOT SIZE TEST.**

   Using a bifocal lens, check that the dimensions of the dot at CTF luminosity conform to CTF recommendations.

   If not, regulate with the focus control.

9. **COLOURS TYPE.**

   Check by sight that all the available colours are displayed in a rectangle at the centre of the screen.

10. **PATTERN TEST.**

    Check by sight that a pattern of "O's" and "H's" are displayed in all the available colours.

6.7 TKEY04: TEST PROGRAM FOR LINE 1 KEYBOARDS

PROGRAM PURPOSE

This program is intended to test line 1 keyboards using a graphic 14" colour display.

HARDWARE REQUIRED

System memory, standard keyboard/video controller with keyboard and monitor, graphic colour video controller and monitor, floppy disk unit controller (TCB and CACHE memory on M60).

PRE-SETTINGS

The operator must connect the keyboard being tested to the graphic, colour Video Display Unit.

All program load and execute operations must be performed on the keyboard connected to the standard VDU controller.

LOADING PROCEDURES

Refer to section 1.3.2

6.7.1 TEST DESCRIPTION

TEST 1: SELF DIAGNOSTIC TEST

The graphic video is reset. The AUTODIAGNOSTIC TEST is started to test the keyboard and if present the ELB. In particular the keyboard is checked to see that it has sent the FC code on line, the line is then reset and a check made for any short circuits between keys.
The autodiagnostic result is read; if the result is negative the program returns to MONITOR, if positive the program continues with the next test.

This test cannot be skipped.

TEST 2: LEDS AND BUZZER TEST

The READY, L1 and L2 LEDs on the keyboard are switched on and off in order a number of times. The status of the LEDs on the graphic display should correspond to that on the keyboard (on = red, off = black).

For the BUZZER test, the operator should ensure that when the VERIFY BUZZER message is displayed, the buzzer does not sound and that when VERIFY BUZZER ON is displayed, it does sound.

This test may be omitted or recycled in the TEST SEQUENCE.

TEST 3: NUMERICAL KEYBOARD TEST

This test checks that the numeric keys are correct and fully operational.

When a key is depressed by the operator, the corresponding key on the graphic display is coloured in and its position code, sent out by the keyboard, is written in the centre.

If the operator hits the same key several times, the colour of the key changes in the following sequence:

red, yellow, blue, magenta, cyan, red...

The test ends after at least one key has been pressed followed by a TIMED OUT period of x seconds, where x is the TIME OUT period set in the pre-program.

This test cannot be omitted.

TEST 4: DIODES STATUS TEST

The diodes which contain information on the keyboard type and origin are read and the relative information displayed.

The operator then checks that keyboard type and origin correspond.

This test may be omitted but NOT recycled in the TEST SEQUENCE.

TEST 5: KEYS TEST

The Keys test is only performed if selected in the pre-program.
Its purpose is to check the operation of the keys; each change of position made by the operator should correspond to the position indicated on the graphic display.

This test may be omitted but NOT recycled in the TEST SEQUENCE.

TEST 6: ALPHABETICAL KEYBOARD TEST

The keys on the alphabetical keyboard are tested as described in test 3,

This test may be omitted but NOT recycled in the TEST SEQUENCE.

STANDARD 15 NUMBERS

The standard 15 number are given below:.

INTERNATIONAL	004
LATIN-FARSI	104
LATIN-ARABIC	105
LATIN-ARABIC	098
GERMANY	127
GERM. DIV 2137	128
PORTUGAL	166
SPAIN	187
SPAIN 2	188
DENMARK	411
FRANCE	435
LATIN-GREEK	462
LATIN-HEBREW	501
ITALY	504
JAPAN	512
NORWAY	609
SWEDEN-FINLAND	684
SWITZERLAND	687
SWITZ. GERMAN	689
SWITZ. ROMANDE	689
USSR	723
UK	729
USA-ASCII	732
USA-OCA	736
YUGOSLAVIA	755

6.7.2 ERROR MESSAGES

The error messages output by the program are listed below:

A) ON STANDARD MONITOR

- *** PRIVILEGED INSTRUCTION TRAP ***

  indicating that a privileged instruction has been executed in user mode.

- *** SEGMENT TRAP ***

  a memory segment not handled by the MMU has been accessed.

- *** NON MASKABLE INTERRUPT ***

  a non-maskable interrupt has been generated.

- THE PRESENT CONTROLLER IN SLOT "X"

  ANSWERS PHYSICAL NAME "YY"

  INSTEAD OF "ZZ"

  indicating that name of controller in slot x is yy and not zz.

- THE SLOT "X" IS EITHER EMPTY OR

  CONTAINS A NOT SELFDECLARING CONTROLLER

  slot x is either empty or controller does not reply present.

- RESET LINE ERROR

  indicating an error in transmission of the line reset command.

- TIME-OUT ERROR (TX)!!

  time allowed for a transmit to keyboard operation has expired.

- TIME-OUT ERROR (RX)!!

  time allowed for a receive from keyboard (return code) operation has expired.

- SELF DIAGNOSTIC ERRORS

  errors have occurred in the autodiagnostic.

- KEYS ALWAYS PRESSED

  a key (switch) code is being sent out repeatedly by the keyboard.

- CODE KEYS ALWAYS PRESSED

  a key code is being sent out repeatedly by the keyboard.

- DIAGNOSTIC RESULT: HARDWARE FAULT

  a summary message indicating that an error has been found in the course of the program.

B) ON GRAPHIC MONITOR

- NOT RECEIVED FC CODE

  indicating that the keyboard has not sent out the FC code following the autodiagnostic.

  The autodiagnostic is carried out only when the system is switched on (when the keyboard is powered).

- RESET LINE ERROR

  indicating an error in transmission of the line reset command.

- TIME-OUT ERROR (TX)!!

  time allowed for a transmit to keyboard operation has expired.

- TIME-OUT ERROR (RX)!!

  time allowed for a receive from keyboard (return code) operation has expired.

- SELF DIAGNOSTIC ERRORS

  errors have occurred in the autodiagnostic.

- LED READY ERROR

  an error in transmission of the command to switch on or off the READY LED.

- LED L1 ERROR

  an error in transmission of the command to switch on or off the L1 LED.

- LED L2 ERROR

  an error in transmission of the command to switch on or off the L2 LED.

- BUZZER ERROR

  an error in transmission of the command to sound the buzzer.

- DIODES STATUS ERRORS

  an error in issue of the command to read the status of the diodes giving information on the type and origin of keyboard used.

- REPEAT FOR EXTRA TIME

  a key has been depressed for too long.

- CONTEMPORANEITY ERROR

  two keys have been depressed simultaneously.

- INCOHERENT CODE XX

  a position code XX not in the set of key codes has been received.

- LED KANA MODE ERROR

  an error in issue of the command to switch on or off the MODE LED of the KATAKANA keyboard.

- LED SHIFT LOCK ERROR

  an error in issue of the command to switch on or off the SHIFT LOCK LED.

- CODE KEY XX

  ALWAYS PRESSED

  a key position code XX is being sent out repeatedly by the keyboard.

- KEYS ALWAYS PRESSED

  a key (switch) code is being sent out repeatedly by the keyboard.

7.1 MULT13: SERIAL CHANNEL MULTIPLEXER TEST PROGRAM

PROGRAM PURPOSE

This program is designed to detect and diagnose Serial Channel Multiplexer errors.

HARDWARE REQUIRED

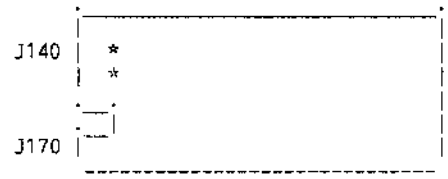
MULTIPLEXER controller (GO322), and a VIDEO/KEYBOARD controller (GO 252) for the specific purpose of loading the Monitor.

NOTE:

The Mux cannot be tested when it has a workstation capable of loading the Monitor connected, as it is impossible to guarantee a correct IPL from disk (when there is a Mux fault).

PRE-SETTING

To test the Serial Channel Multiplexer in Current Loop or RS232 connection, the DIP-switches must be set as required. The position of the switches on the board is shown by an asterisk *, the upper being the switch for LINE 1, the lower for LINE 3.



When a switch is set in position 10, the channel is in Current Loop; with the switch in position 5, the channel is in RS232.

LOADING PROCEDURES

Refer to section 1.3.2.

7.1.1 TEST DESCRIPTION

TEST 1 - MUX SLOT TEST

Checks that a given slot contains the correct controller board. This test cannot be omitted.

TEST 2 - VER. FLAGS & CONTENTS D.P.MEMORY

Checks that the Multiplexer board signals it is free after the power-on autodiagnostic.

TEST 3 -DUAL PORT RAM TEST FROM Z8000

Checks for shorts between bytes or addresses of the Dual-Port RAM and also memory bank selection by Olibus.

TEST 4 - SHORTS/STUCK DUAL P.RAM:FROM Z80

Similar to the previous test, but in this case the Mux internal Dual-Port RAM is tested in relations with the Z80.

TEST 5 - SHORTS/STUCK INTERNAL RAM:FROM Z80

Test 5 checks operation of the board internal RAM (not Dual-Port) storage, used by the Z80 as stack pointer, receive buffer or for routine operations.

TEST 6 - READ INTERRUPT VECTOR PORT

Checks interrupt vector writing on the vector port. The test is not performed directly by Olibus but through a specific command forcing the Mux Z80 to fetch and write on the vector port the vector set by the Z8000 in the Dual-Port RAM. When this has been done, the Z8000 reads the port through a normal I/O operation without resorting to an interrupt.

TEST 7 - SPECIAL INTERRUPT TEST

Checks the special interrupt (vector 3E) by way of a program command. With no interrupt vector loaded earlier, the Z80 can generate a vectored interrupt with fixed vector "3E". The Z8000 then tests the special interrupt vector.

TEST 8 - CTC TEST

Checks that the CTC's 1 and 2 are programmed correctly. The TIMEO-TIME1 output is then checked using routines written into the Dual-Port RAM by the Z8000 and performed by the Z80 to program the CTC and DART devices. The CTC's are also used to check operation of the circuit generating the signal DIV80 on a TRCTC signal (board clock).

TEST 9 - VERIFY SWITCH OF CURRENT LOOP/RS232

Checks that the SEL31 and SEL11 jumpers (DIP-switches) are set correctly and as declared at the start of the program. The test is made on the two DART devices, with the DIAG set "0" for shifting on SEL13 and SEL31, by

reading the register RR0 which monitors the status of control signals DCD, CTS and RI.

TEST 10 - DART: DIAGNOSTIC LOOP TEST

Checks the two DART devices in diagnostic loop (diag = 1) with interrupts disabled. The diagnostic clock generated by the Z80 is used and transmission/reception occurs on the same DART channel (TXD10, for example, will be looped on RXD10). Both channel A and channel B (in Current Loop) are tested and the number of characters transmitted is limited.

7.1.2 ERROR MESSAGES

The probable cause of any error is the multiplexer controller, if changing this fails to clear the error try changing the video/keyboard controller.

7.2 MULT22: SERIAL CHANNEL MULTIPLEXER TEST PROGRAM

PROGRAM PURPOSE

The purpose of the program is to test the Serial Channel Multiplexer and diagnose any errors.

HARDWARE REQUIRED

MULTIPLEXER controller (G0322) and a video/Keyboard controller (G0252) to load the Monitor.

WARNING

This program can be run only when the video/keyboard group is integrated and not of the workstation type as, for this test, loop plugs are placed on the J170 connector or the D-Box.

N.B.

This program is to be run only after successfully completing the tests of the MULTI12 program.

PRESETTING

Refer to corresponding section in the MULT13 PROGRAM (7.1).

LOADING PROCEDURE

Refer to section 1.3.2.

7.2.1 TEST DESCRIPTION

Before commencing tests the MULT13 program (where tests 1 to 10 are found) should be successfully completed.

TEST 11 - DAISY-CHAIN INTERR.PRIORITY TEST

The section of the board daisy chain relating to the CTC devices, and priority for the CTC and DART channels is checked. Priority is from "0" down to "3". The CTC in position R09 has higher priority than the one in position P09 and, for the DART devices, channel A is the priority channel. With DIAG at 1, the channels are loaded, checking that all interrupts are handled in the normal way (through the vectors, it should be able to distinguish between the interrupting channels).

TEST 12 - DART: EXTERNAL LOOP TEST

DART 1 is programmed for transmission via the loop plug when the jumpers and plug are found to correspond. The transmitted data is checked with data received.

Initially the test is run on channel B only; channel A is subsequently tested when fitted with the appropriate plug.

A similar sequence is run on DART 2.

7.2.2 ERROR MESSAGES

The probale cause of any error is likely to be the multiplexer controller, if changing this fails to clear the fault try changing the video/keyboard controller.

7.3 WSVID6: STANDARD VDU TEST PROGRAM

PROGRAM PURPOSE

The program is designed to check that the Keyboard and Video hardware modules are working correctly and is valid only on standard video display units with ELB 3684 o WS685/M workstations on Line 1 products.

HARDWARE REQUIRED

MULTIPLEXER controller (G0322) and Floppy Disk controller.

GENERAL

There are 4 phases to the test:

a) Workstation self-diagnostic test.

b) Workstation service channel loop test with test pattern transmitted and received.

c) Character set stored in ROM displayed and checked including SCROLL operation check.

d) Test patterns displayed and checked, with adjustments facilities for correction (if necessary).

NOTES

When the program is set for AUTOMATIC execution, picture scrolling is controlled by timing from a software timer.

Tests can be selected using the Monitor HELP facility.

WARNING

The program can only run if the correct SET-UP parameters are entered in the preprogram. These parameters can be obtained by acceessing the WS SET-UP pages.

SET-UP ACCESS PROCEDURES

1. Switch WS off.

2. Set LOCAL ON/OFF switch to LOCAL position.

3. Switch WS on again.

4. Hit ENTER to select the SET-UP pages (selected by default, otherwise use SKIP key to point to SET-UP then hit ENTER).

5. Hit SKIP a number of times until the SET-UP B page is displayed.

6. Note the parameters for SERIAL H line (displayed by default).

With the 9" monitor, the operator can display the 0 pattern in two formats by entering or exit entering as appropriate:

0 = Exit
1 = 520 character format
2 = 2000 character format

Luminosity can thus be checked in the two formats.

TEST 8 - PHOTOMETRIC TEST

Test 8 sets the video in reverse; using a photometer, the operator takes readings in the 4 corners and the centre of the screen and checks that they are within the technical specification recommendations.

A 5 cm square is then displayed in the centre of the screen in reverse; again using the photometer, the operator checks luminosity.

If ENTER is pressed, a second square of the same size is displayed in high luminosity beside the first. Luminosity should be uniform and correspond to the technical specification recommendations.

SKIP should be pressed to return to the original picture. This operation should be performed several times to give optimum luminosity.

TEST 9 - DYNAMIC DISTORTION TEST

In test 9, two rectangles, proportional in length and size to the type of video, are displayed, with their lesser side on the screen left margin. Equidistant, vertical lines are drawn to the right of the screen. After increasing luminosity by way of the brightness potentiometer, the operator should check that any distortion is within technical specification recommendations.

7.3.2 ERROR MESSAGES

The error messages for this test are divided into the following five groups (groups 1 to 4 are displayed on the local WS and group 5 on the remote WS):

1) BLOCKING ERRORS

***** PRIVILEGED INSTRUCTION TRAP *****
***** SEGMENT TRAP *****
***** NON MASKABLE INTERRUPT *****
If these messages are displayed, the system should be reset.

2) MULTIPLEXER ERRORS

THE PRESENT CONTROLLER IN SLOT XX
ANSWERS PHYSICAL NAME YY
Displayed if a contoller other than the one expected is found.

THE SLOT XX
A NOT SELFDECLEARING CONTROLLER
Here, the slot polled responds empty or has a controller which does not identify itself.

LINE CONFIGURATION ERROR
This is a hardware error attributed to the controller during initialization.

3) MUX/DEMUX/W.S. ERRORS

UNAVAILABLE W. S. ERROR
The workstation being tested is either not on line or is off.

BUFFER NOT EMPTY ERROR
After the autodiagnostic string has been read, the circular deposit buffer still contains some characters. A workstation hardware error.

CONTROL CHANNEL INIT. ERROR
Displayed when the workstation service channel cannot be programmed. MUX/workstation hardware error.

CONTROL CHANNEL RD/WR ERROR
This error can be attributed to:
workstation malfunction; workstation and DEMULTIPLEXER electric connection fault; malfunction of the workstation autodiagnostic request channel

KEYBOARD/VIDEO CHANNEL INIT. ERROR
The video/keyboard channel has not been initialized correctly. A MUX/workstation hardware error.

KEYBOARD/VIDEO CHANNEL RD/WR ERROR
This error can be attributed to:
workstation malfunction; workstation DEMULTIPLEXER electric connection fault or workstation video/keyboard channel hardware error.

KEYBOARD TRANSP. CHANNEL INIT. ERROR
Keyboard channel incorrectly programmed in transparent mode. MUX/workstation hardware error.

KEYBOARD TRANSP. CHANNEL RD/WR ERROR
This error can be attributed to:
workstation malfunction; workstation-DEMULTIPLEXER electric fault or workstation transparent keyboard channel hardware error

REMOTE LOOPBACK ERROR
This error can be attributed to electric connections between MUX, D-BOX, T-BOX and workstation on the workstation service channel.

HARDWARE W. S. ERROR
This error can be attributed to MUX, D_BOX, T_BOX and workstations on all channels in the read/write phase (data read from workstation and commands written to workstation).

4) WORKSTATION OR VIDEO/KEYBOARD ERRORS FOUND IN AUTODIAGNOSTIC

VIDEO RAM TEST ERROR RAM 1 or 2 of the video faulty.

VIDEO NOT PRESENT ERROR Video not connected.

VIDEO TEST ERROR Video hardware error.

Program execution is terminated if these errors arise.

For errors found in the video regulation tests, the operator should proceed as instructed in the tests.

1. **SELF W.S. RESULT FAULT**
   Non-blocking hardware error found on workstation in autodiagnostic. The hardware fault is not in the video assembly so all the tests relating to the video may still be carried out.

2. **SIO 1 CHANNEL B TEST ERROR**
   Hardware error on the SIO dedicated to workstation keyboard exchanges.

3. **KEYBOARD NOT PRESENT**
   The keyboard is not connected.

4. **SELF KEYBOARD TEST ERROR**
   Error found in the keyboard autodiagnostic phase.

5) ERRORS ON REMOTE WS

- SELF DIAGNOSTIC WS TEST ERROR
- REMOTE LOOPBACK TEST ERROR
- SCROLLING CHAR. AND SET ATTR. TEST ERROR
- SCREEN SIZE TEST ERROR
- GEOMETRY AND LINEARY TEST ERROR
- SPORT SIZE TEST ERROR
- LUMINOSITY TEST ERROR
- PHOTOMETRIC TEST ERROR
- DYNAMIC DISTORTION TEST ERROR

7.4 WSKEY6: STANDARD WORKSTATION KEYBOARD TEST PROGRAM

PROGRAM PURPOSE

The program is designed to check the operation of standard ELB 3684 or the multifunctional workstation connected to the WS685/M for Line 1 MOS products.

HARDWARE REQUIRED

MULTIPLEXER controller (G0322) and Floppy Disk Controller.

WARNING

The program can only run if the correct SET-UP parameters are entered in the preprogram. These parameters can be obtained by accessing the WS SET-UP pages. Refer to WSVID6 program section 7.3 for WS SET-UP access procedures.

LOADING PROCEDURE

Refer to section 1.3.2.

7.4.1 TEST DESCRIPTION

TEST 1 - WORKSTATION AUTODIAGNOSTIC RESULT CHECK

Refer to TEST 1 of the WSVID6 program (section 7.3.1).

TEST 2 - CHECK OF CONNECTION BETWEEN WORKSTATION AND MUX

Refer to TEST 2 of the WSVID6 program (section 7.3.1).

TEST 3 - LED BUZZER CHECK

Checks that when the workstation is switched on the POWER ON LED (non present on WS 685/M lights up. The workstation is then switched on and off three times with an interval of one second; the buzzer should operate each time. The three LEDs are then checked by switching them on in a binary sequence from 000 (LEDs all off) to 111 (LEDs all on).

TEST 4 - POSITION CODE CHECK

A picture of the keyboard being tested, valid for all types of keyboard connected to the workstation, is displayed on the video.
If the video connected is a 5" video (discovered from autodiagnostic data), the test will be omitted. It may be replaced, however, by some of the workstation LOCAL features (see section on WORKSTATION KEYBOARD LOCAL TEST).

CHECKING POSITION CODES OF KEYS

When a key on the keyboard is depressed, the corresponding key of the keyboard displayed on video is set in reverse and the current module 100 counter, representing the number of times that particular code has been received, is displayed inside. The software provides the test-end timer with the time in minutes and seconds.

The operator must check for correspondance between the key depressed and the key set in reverse on the screen; where they do not correspond, the operator should look into the source of error.

REPEAT KEY CHECK

Here, the operator maintains the REPEAT key depressed, presses any other key and checks that the internal counter value is incremented accordingly.

CHECKING SHIFT KEY, SHIFT LOCK KEY AND RELATIVE LED

When the SHIFT LOCK key is depressed, the LED indicating capital letter code output should come on; when the SHIFT key is depressed subsequently, the LED should go off. This operation should be performed a number of times for a thorough check.

TEST EXECUTION END

The test ends when one of the following events occurs:

a) a time-out

b) the repeat code for extra time is sent out on line 20 times; this can be attributed to a short circuit on one or more keys

c) the keyboard being tested is not the one dedicated to the monitor, and an appropriate monitor command is entered via the monitor keyboard.

NOTE

This test should be included in the test sequence so that operation of the ENTER key can be checked before moving on to the subsequent tests.

TEST 5 – SWITCH-KEY STATUS CHECK

In this test, the operator sets the keys in all positions, left and right, horizontal and vertical, and checks that the arrows displayed on the video correspond to the positions of the switch-keys on the keyboard.

The test is terminated following the operation of the ENTER key on the keyboard being tested or a program time-out (30 seconds).

TEST 6 - APPLICATION ENVIRONMENT AND COUNTRY

In this test, both the relative national version and the keyboard type, in relation to the application environment, are displayed by reading the status of the diodes on the keyboard.

This test checks only effectiveness of the diodes, as it is assumed that the positions of the characters on the keys and the type of application environment have not been altered.

The operator checks that the application environment, country and standard displayed correspond to those of the keyboard being tested. The test is terminated after the operator depresses ENTER on the keyboard being tested or after a programmed time-out (30 seconds).

7.4.2 ERROR MESSAGES

The error messages for this program are as listed in the WSVID6 program, section 7.3.2, with exception of the REMOTE WS error messages which are NOT relevant and the addition of the following messages:

HARDWARE KEYBOARD ERROR
Keys transmit identifier code only on line.

KEY ALWAYS PRESSED ERROR
Repeat over-time error. Output when the keyboard is enabled to send out position codes on line and the same position code is received non-stop.

INCOHERENT CODE ERROR
Incoherent position code received. Output when an unexpected position code is received from the keyboard being tested - can occur following a short between two or more keys.

DIODES STATUS ERROR
The application environment and country diodes read incorrect status.

REFUSED CHANNEL COMMAND ERROR
The error may be attribuited to the MUX; the command end interrupt was not sent out during the sospension (ker_readev) and comand is therfore aborted.

SCREEN SIZE INCOHERENT
The video connected to the workstation is 5", or the video type has been incorrectly read. Tests 3, 4 and 5, requiring a drawing of the video on the screen, are omitted.

A POSITIONAL CODE HAS NOT BEEN RECEIVED IN TEST FOUR
The position codes have not been received. The message is output if no position code is received in the time set for parameter acquisition - no key has been depressed by the operator or there may be a error in the hardware of the keyboard being tested.

TEST FIVE NOT EXECUTED BECAUSE
KEYS HAS NOT BEEN SELECTED
Test 5 has been included in the default test sequence though the switch-keys feature was not requested in the pre-program.

TEST SIX NOT EXECUTED BECAUSE
ALPHABETIC KEYBOARD NOT PRESENT
The test has not been carried out because the status of the application environment and country decoder diodes is %FF.

7.4.3 WORKSTATION LOCAL KEYBOARD TEST

GENERAL

This test checks that the characters are in their correct positions on the keyboard and that the keyboard is, therefore, one of the national versions that can be used with the workstation.

The position of the characters is checked by comparing a mask of seriographs of the appropriate national keyboard and the layout of the keyboard being tested.

An entire set of the seriograph character masks should be available.

No program is required in this test phase as the check is made with the workstation in LOCAL.

WARNING

It is important that the workstation is in LOCAL before it is switched ON; if it is already ON, it should be switched OFF, set in LOCAL and switched ON again.

PROCEDURE

Set the WS to LOCAL by operating the LOCAL switch and then switch ON the supply. Position the cursor on LOCAL, hit ENTER. Then position the cursor on DVCS and hit ENTER again. The operator is then required to hit each key on the keyboard and verify that the key hit corresponds to the character displayed.

NOTE

This test cannot be used for LATIN/ARABIC keyboards. In such cases only a visual check can be made where the keyboard layout is compared with the seriograph masks.

7.5.2 ERROR MESSAGES

The error messages for this program are as listed in the WSVID6 program, section 7.3.2, with exception of the messages associated with the REMOTE WS, PIN-PAD and CARD READER which are listed below:

SIO 3 CHANNEL B TEST ERROR Hardware error detected on SIO channel B dedicated to WS PIN-PAD communi- cation.

PIN-PAD NOT PRESENT ERROR The PIN-PAD keyboard is not present.

PIN-PAD CHANNEL INIT. ERROR The PIN-PAD channel has not been initialized.

PIN-PAD CHANNEL RD/WR ERROR This error may be caused by:
Faulty operation of the Work Station; electrical connection between WS and DEMULTIPLEXOR or hardware error on the WS PIN-PAD channel.

RECEIVED CODE ERROR Error detected during a read of the code generated by pressing the keys of the PIN-PAD.

BOARD PIN-PAD/CARD READER ABSENT The PIN-PAD/CARD READER board is not present on the WS.

SIO 3 CHANNEL A TEST ERROR Hardware error detected on SIO channel A dedicated to WS CARD READER communication.

CARD READER NOT PRESENT ERROR The CARD READER is not present.

CARD READER CHANNEL INIT. ERROR The CARD READER channel has not been initialized.

CARD READER CHANNEL RD/WR ERROR This error may be caused by:
Faulty operation of the Work Station; electrical connection between WS and DEMULTIPLEXOR or hardware error on the WS CARD READER channel.

START UNKNOWN ERROR This is displayed if the START code has not been found during the CARD READER read operation.

STOP UNKNOWN ERROR This is displayed if the STOP code has not been found during the CARD READER read operation.

CARD READER ALWAYS INSERTED ERROR This shows that the card is permanently inserted in the unit under test.

NOT RECEIVED DATA Card read error.

ERRORS ON REMOTE WS

- SELF DIAGNOSTIC WS TEST ERROR
- REMOTE LOOP BACK TEST ERROR
- LEDS PIN-PAD TEST ERROR
- KEYBOARD PIN-PAD TEST ERROR
- CARD READER TEST ERROR
- CARD WRITER/READER MRW1810 TEST ERROR

7.6 WSLIN3: MUX - ELB 3683 CONNECTION TEST PROGRAM

PROGRAM PURPOSE

This program is intended to check the physical and logic connection between the MUX (G0322), D-BOX and WORK STATION (ELB 3683).

HARDWARE REQUIRED

FLOPPY DISK CONTROLLER and MUX controller (G0322).

WARNING

The program can only run if the correct SET-UP parameters are entered in the preprogram. These parameters can be obtained by accessing the WS SET-UP pages. Refer to WSVID6 program section 7.3 for WS SET-UP access procedures.

LOADING PROCEDURE

Refer to section 1.3.2.

7.6.1 TEST DESCRIPTION

INITIALIZATION PHASE

The operations described below are performed in initialization:

- The MUX board slot is tested, the results analysed and any errors signalled
- A reset command is issued to the MUX, and a time allowed for the processor on board (Z80) to complete operations
- The MMU is programmed so that the dual-port memory on the MUX board becomes accessible to the CPU (Z8001).

TEST 1 - CHECKING THE CONNECTION BETWEEN MUX, D-BOX AND WS

In test 1, the following operations are performed:

- The MUX line (1..4) associated with the WS being tested is programmed with the SET UP parameters
- The service channel and the video/keyboard channel are initialized with the default parameters

- A REMOTE LOOPBACK command is issued. Execution of this command entails creation of a logic loop of the WS (channel 0) on the main line of the MUX. The loop is used for sending the data string received at the end of the command to the host. The string received is compared to the string transmitted. If the two are not identical, program execution ends and a diagnostic message is displayed.

The test may be omitted but cannot be recycled.

TEST 2 - ANALYSING THE AUTODIAGNOSTIC RESULTS AND THE WS CONFIGURATION

In test 2, the data string compiled by the WS firmware during the autodiagnostic tests is checked. Particular attention is given to the bytes relating to the video tests. If the results are not satisfactory, program execution ends and a diagnostic message is displayed.

It is important for the WS to be switched OFF and on again before an attempt is made to run the program so as to have a fully up to date autodiagnostic picture.

The test may be omitted but cannot be recycled.

7.6.2 ERROR MESSAGES

The error messages for this program are as listed in the WSVID6 program, section 7.3.2, with exception of the REMOTE WS messages which are NOT significant and the addition of the following messages:

END COMMAND ERROR
Error in the end of command signal issued by the MUX. The error can be attributed to the MUX, D-BOX, T-BOX and WS on all channels during the RD/WR phase (data read from WS and commands written to WS).

VIDEO SIGNALS TEST ERROR
Hardware error of the video management signals.

If these errors occur, program execution will be terminated.

7.7 PRMUX0: PRINTER VIA MUX OR ELB 3683 TEST PROGRAM

PROGRAM PURPOSE

This program verifies the correct physical/logical connection and, therefore, the correct operation of the MUX, the D-BOX, the Work Station and the printer.

HARDWARE REQUIRED

Floppy/mini-floppy disk controller, display-keyboard controller, MUX controller T-BOX, D-BOX, hardware loop plug, printer.

PRELIMINARY OPERATIONS

The following connections should be made on the loop plug:

Link pin 2 to pin 3
Link pin 4 to pin 5 and to pin 8
Link pin 6 to pin 20

LOADING PROCEDURES

Refer to section 1.3.2.

7.7.1 TEST DESCRIPTION

The testing procedure followed in this program is set out below:

INITIALIZATION

Initially MUX board is checked to see if it is in the correct slot position as selected by the operator. Then a reset command is sent to the MUX and the program waits for the Z80 on the MUX board to complete initialization. The MMU is then programmed to allow the CPU Z8000 to access the dual-port memory on the MUX board.

PROGRAMMING THE PRINTER

The MUX is programmed to communicate with printers jumpered XON-XOFF (DC1-DC3) and does not handle breaks. The printer DIP-switches must correspond to the parameters set by the operator to prevent printing or to ensure that the printer prints correctly.

TEST 1 TEST OF MUX AND D-BOX CONNECTION IN TRANSPARENT MODE

A loop plug must be connected for this test. The MUX line dedicated to the printer is programmed with the following parameters:
19200 baud, 8 data bits, 1 stop bit, no parity bit.
The test consists in transmitting a data buffer and waiting for the end of transmission signal and the signal indicating that the data is available in the receive buffer. The two buffers are then compared. If an error is detected, the program terminates execution and displays the relevant diagnostic messages.

As specific hardware is necessary for this test, it is not included in the normal test execution cycle; thus no request is made for this test during the set parameters phase. To execute this test, the operator must set the number of cycles required each time before launching the test program.

TEST 1 WORK STATION STATUS TEST

This test is an alternative to the previous test, and is run for non-transparent printer connection, i.e. connection via a work station.
The test is run by programming the line selected by the operator with the SET-UP parameters of the work station (ref. to WSVID6 program for SET-UP ACCESS procedures). The communication channels are initialized and the program reads the state of the autodiagnostics by means of a specific command from the work station. It is advisable to switch the work station off and on again to update its status.
This test can be repeated but not skipped.

TEST 2 PRINT OF THE PRINTER GRAPHIC SET

The whole graphic set of the printer (ISO characters) is printed out. The operator must check that the printing is correct.
This test can be repeated or skipped.

TEST 3 PRINT OF THE CIRCULAR BUFFER

The MUX line and the RS232 channel selected by the operator are programmed and a print out of a buffer containing a test pattern is obtained. The operator must check that the printing is correct.
This test can be repeated or skipped.

TEST 4 HORIZONTAL ALIGNMENT TEST

A line of "_" characters is printed. The operator must check that the characters printed are correctly aligned horizontally.
This test can be repeated or skipped.

TEST 5 VERTICAL ALIGNMENT TEST

A line of "E" characters is printed. The operator must check that the characters printed are correctly aligned vertically.
This test can be repeated or skipped.

TEST 6 HORIZONTAL SPACING TEST

A line of "H" characters is printed. The operator must check that the spacing between the characters printed is correct.
This test can be repeated or skipped.

TEST 7 LINE FEED PITCH TEST

A line of "E" characters is printed, then a line feed command is issued, and then another line of "E" characters is printed. The operator must check that the spacing between the lines printed is correct.
Note that the line feed is 5.08 mm for 1/5 inch pitch, and 4.23 mm for 1/6 inch pitch.
This test can be repeated or skipped.

TEST 8 DIRECTION OF PRINT HEAD MOVEMENT TEST

Four lines of "E" characters are printed. The operator must check that the print head moves correctly.
This test can be repeated or skipped.

TEST 9 CORRECT EXECUTION OF PAGE CHANGE TEST

Four lines of "E" characters are printed and the page is changed. The operator must check that the operation is performed correctly.
This test can be repeated or skipped.

7.7.2 ERROR MESSAGES

Below is a list of error messages used in the various tests. The messages which are not self-explanatory are followed by a brief explanation.
The error messages can be divided into the following groups:

a) **BLOCKING ERRORS**

Refer to ERROR MESSAGES of the WSVID6 program (section 7.3.2 part 1)).

b) **ERRORS CAUSED BY THE MUX BOARD**

Refer to ERROR MESSAGES of the WSVID6 program (section 7.3.2 part 2)).

c) **ERRORS CAUSED BY THE PRINTER**

UNAVAILABLE PRINTER ERROR
The printer is not connected to the line or is off.

PRINTER OFF
The printer is off or its connector is not plugged in.

NO CONNECTION D_BOX - PRINTER
The printer is not connected to the D-BOX.

NO CONNECTION W.S. - PRINTER
The printer is not connected to the Work Station.

ERRORS INVOLVING HARDWARE CONNECTIONS AND TRANSMISSION CHANNELS

REMOTE LOOP BACK ERROR
The external loop plug is not jumpered correctly.

CHANNEL INITIALIZATION ERROR

CONTROL CHANNEL INIT. ERROR
The Work Station channel was not initialized due to MUX/W.S. hardware problems.

CONTROL CHANNEL RD/WR ERROR
Error occurring during the Work Station autodiagnostics. Check the connection between the Work Station and the D-box.

LINE ERROR
An error has occurred on the transmission line. Check the connection between the D-box and the Work Station.

CHANNEL ON READ ERROR
Line error occurring while receiving from a peripheral.

CHANNEL ON WRITE ERROR
Error occurring because the transmission channel is not available or because the transmission buffer is not large enough.

ERRORS INVOLVING THE WORK STATION

UNAVAILABLE W.S. ERROR
The Work Station is not available, it is either switched off or not connected.

KEYBOARD/VIDEO CHANNEL INIT. ERROR
The video/keyboard channel of the Work Station has not been initialized due to hardware problems.

VIDEO NOT PRESENT ERROR
The video is not connected to the Work Station.

VIDEO TEST ERROR

SELF KEYBOARD TEST ERROR

SIO1/SIO2 CHANNELS A/B ERROR
An error has been detected in the interface of channels A and B of the Work Station.

HARDWARE W.S. ERROR

d) **ERRORS INVOLVING THE TRANSMIT AND RECEIVE BUFFERS**

BUFFER RX EMPTY ERROR
The receive buffer is empty. If this message is displayed during Test 1, check the hardware loopback jumper settings, otherwise it means that the printer is faulty.

BUFFER RX NOT EMPTY ERROR
The receive buffer still contains characters. A hardware error has occurred involving the MUX or the printer.

BUFFER RX OVERFLOW ERROR

COMPARE DATA RX ERROR
The data contained in the transmitted buffer is not the same as the data in the received buffer. Check the electrical connection between the MUX, T-BOX and D-BOX.

e) **OTHER ERRORS**

END COMMAND ERROR
While waiting for the end command, no interrupt was generated and the command was aborted.

NO EXIT NMI DURING RESET PHASE
The reset was not executed.

INCOHERENT ERROR MESSAGE REPEAT TEST
This message is displayed if an error which is not included in the functional checks program occurs.

8.1 GLAV28: GLAV 24 TEST PROGRAM

PROGRAM PURPOSE

The program is designed to check the GLAV 24 board.

HARDWARE REQUIRED

Glav 24 board (60300), hardware plug.

SETTINGS

A hardware plug is required in order to carry out a full test on the CTC device and on the V24 interface output signals. The plug should be set in the following way:

Connect pins
1-A 2-B 3-CD
E-H 6-J 4-K

LOADING PROCEDURE

Refer to section 1.3.2.

8.1.1 DESCRIPTION OF TESTS

The program is divided into functional checks to test the controller.

It should be noted that when no plug is present, the V24 interface signals are not tested and the CTC device test is not complete.

Test 1 checks the operation of the controller bus.

Test 2 is a check on the operation of the 8253 chip.

Test 3 checks that the CTC is functioning correctly (the loopback plug is required to carry out this test fully).

Test 4 checks the SIO by transmitting a character buffer in asynchronous protocol using a diagnostic loop.

Test 5 checks the SIO by transmitting a character buffer in BSC protocol using a diagnostic loop.

Test 6 tests the SIO by transmitting a character buffer in SDLC protocol without diagnostic loop.

Test 7 is a check on NRZI modulation and demodulation.

Test 8 checks the PLL section.

Test 9 checks the buffers and line signals by transmitting a character buffer in SDLC protocol without diagnostic loop (with the plug inserted).

This test may be missed out (as indicated by the "?" sign in the test list), if the plug is not present (the diagnostic loop is used to continue tests).

Test 10 checks transmission by making the transmit clock loop back via the plug and using it as the receive clock.
This test can also be missed out as in test 9.

8.1.2 ERROR MESSAGES

The messages are made up of a first line indicating the type of error, and, where possible, a second and third line showing the signals which may have caused the error. Some of messages also give the transmitting frequency at the time of the error.

The information provided in the messages depends on the diagnostic level used; with diagnostic level 1, the message describes the type of error, while levels 2 and 3 provide information on the lines which may be involved in the error.

The majority of the error messages listed below refer to the GLAV24 controller therefore if an error occurs try changing this board first.

The error messages are listed below:

BUS TEST:

- ERROR DATA-BUS
  SIGNALS IOGON, EASTC, RWGOB
  NOS1N, ASTRB11, RDOON

- ERROR SIO-BUS
  SIGNALS SS1ON, IAD10-20, DB00-07
  M100A, IORQB, RD00A, F1Z81
  SES1N, AD011-21, AF001-71
  M100N, IORQN, RD00N, OSC10

- ERROR CTC-BUS
  SIGNALS SCTCN, IAD10-20, DB00-07
  M100A, IORQB, RD00A, SECTC
  AD011-21, AF001-71, M100N
  IORQN, RDOON

- ERROR 8253-BUS:
  SIGNALS S825N, IAD10-20, DB00-07
  SE53N, AD011-21 ,AF001-71
  IORDN, IOWRN

8253 TEST:

- ERROR ON ALL THE CHANNELS
  SIGNAL OSC12N

- ERROR ON CH.0
  SIGNALS OSC12N, P1U40, P011

- ERROR ON CH.1
  SIGNAL OSC12N

- ERROR ON CH.2
  SIGNALS OSC12N, P1U40, P011

CTC TEST:

- DAISY-CHAIN ERROR
  SIGNAL error IE0B1, IE10A, IE1A1, IE1B1
  INCT1, IEO10, INCTN, INTRB, INTAN

- NOT OCCURRED INT. OF CTC-CH. 0, 1, 2, or 3

- ERROR COUNTER CAN.0 - FREQ.:
  VERIFY PATH FROM 8253-OUT2 TO CLK0-CTC

- ERROR COUNTER CAN.2 - FREQ.:
  SIGNALS A1110, A111A, A1112, A1250, A125A

- ERROR COUNTER CAN.3 - FREQ.:
  SIGNALS A1080, A108A, A1082, A1070, A107A

- ERROR COUNTER CAN.1 - FREQ.:
  SIGNALS CXTA0, CXTAA

- INTERRUPT ERROR OF CH.0
  NO OUTPUT OF INTERRUPT VECTOR

- INT. ACK. AND INT. VECTOR ERROR
  SIGNALS VINTA AND VECTN, INTRN AND INTR1

- ERROR ON LOCAL LOOPBACK TEST
  SIGNALS A141O, A141A, A1420, A142A

- STRING TRANSMISSION ERROR CH.A
  SIGNALS TXDA0, TXDAA, TDAS0, A1030, A1042
  CKRAA, CKTAA, A1043, LOAD0

SIO BSC TEST, PLL TEST, SIO ASYNC TEST:

- NOT EXPECTED INTERRUPT FROM CH.B

- CH. A CTS-ON INTERRUPT NOT OCCURRED
  CTS SIGNAL A106B; A105N, LOAD0

- CH. A TX UNDERRUN/END OF MESSAGE

- CH. A CRC/FRAMING ERROR NOT EXPECTED

- CH. A RECEIVE OVERRUN ERROR

- CH. A PARITY ERROR

- CH. A DCD-ON INTERRUPT NOT OCCURRED
  DCD SIGNAL A109B; LOAD0, A105N

- CH. A CTS-OFF INTERRUPT NOT OCCURRED
  CTS SIGNAL A106B; A105N, LOAD0

- CH. A DCD-OFF INTERRUPT NOT OCCURRED
  DCD SIGNAL A109B; LOAD0, A105N

- SYNCHRONISM INTERRUPT NOT OCCURRED
  SIGNALS TXDA0, TXDAA, TDAS0, A1030, A1042
  CKRAA, CKTAA, A1043, LOAD0

- CH. A END OF TRANSMISSION NOT VERIFIED
  SIGNALS TXDA0, TXDAA, TDAS0, A1030, A1042
  SIGNALS CKRAA, CKTAA, A1043, LOAD0

SIO SDLC TEST, PLUG TEST, NRZI TEST, CKRK EXT TEST:

- NOT EXPECTED INTERRUPT FROM CH.B

- DCD-ON INTERRUPT NOT OCCURRED CH.A
  SIGNALS LOAD0, A105N, A1090, A109A, A109B

- CTS-ON INTERRUPT NOT OCCURRED CH.A
  SIGNALS A1060, A106A, A106B, LOAD0, A105N,
  A105A, A1052

- CTS-OFF INTERRUPT NOT OCCURRED CH.A
  SIGNALS LOAD0, A105N, A105A, A1052, A1090,
  A109A, A109B

- SYNCR-ON INTERRUPT NOT OCCURRED CH.A
  SIGNALS TXDA0, TXDAA, TDAS0, A1030, A1042
  A1043, RXDA0, CKRAA, CKTAA
  TXDA0, TXDAA, TDAS0, A1030, A1031
  A103A, A104N, A1042, A1043, RXDA0

- END OF TX NOT OCCURRED CH.A
  SIGNALS TXDA0, RXDA0, CKTAA, CKRAA

- STRING TRANSMISSION ERROR CH.A

- DCD-OFF INTERRUPT NOT OCCURRED CH.A
  SIGNALS A1060, A106A, A106B, LOAD0, A105N,
  A105A, A1052, A1090, A109A, A109B

- ABORT/SEQUENCE ERROR CH.A

- TX UNDERRUN ERROR CH.A

- CRC ERROR CH.A

- RX OVERRUN ERROR CH.A

- NRZI MODULATION ERROR
  SIGNALS A1042, CKRA0, A1043, RXNRZ, DAPAN
  NRZA0, A1050, CKTA2, TDAS0, TXDAA

- PLL ERROR
  COMPONENTS SML5, PMP3, CTL4, NEB1.C, NEB1.D
  NEB1.E AND THEIR SIGNALS

- EXTERNAL RX CLOCK ERROR
  SIGNALS A113N, A1131, A1150, A115A

8.2 LCUX26: LCUX24 DIAGNOST6C TEST PROGRAM

PROGRAM PURPOSE

To provide a diagnostic aid for fault finding on the LCUX24 controller.

REQUIRED HARDWARE

LCUX24 controller.

PRELIMINARY OPERATIONS

To test the line drivers (TEST 6) it is necessary to connect an external loop through a plug mounted on the controller board output connector or at the output of the controller signal cable.

The controller board plug should be connected as follows:

PIN 1 to PIN 2	PIN 6 to PIN 13
PIN 3 to PIN 4	PIN 8 to PIN 15

LOADING PROCEDURE

Refer to section 1.3.2.

8.2.1 TEST DESCRIPTION

TEST 1

The function of the controller BUS is tested by writing an interrupt vector on register 2 of the SIO channel B, reading the same interrupt, writing and then reading specific values in the CTC and 8253 counters.

TEST 2

Each channel of the 8253 component is tested by verifying that after a set time the counter has a value less than half of its initial value.

TEST 3

Each channel of the CTC is tested in timer mode and then in counter mode and after each test the generation of the correct interrupt is verified. Also the funtion of the daisy-chain is verified.

TEST 4

The 2 channels of the SIO are tested by transmitting a string of characters in BSC protocol and using a dianostic loop to test the data transmitted.

TEST 5

The 2 channels of the SIO are tested by transmitting a string of characters in SDLC protocol using the diagnostic loop to test the data transmitted.

TEST 6

The SIO channels are tested by transmitting a string of characters in SDLC protocol without using the diagnostic loop, but using the external loop connector to test the data transmitted. Before commencing the test a check is made to see if PLUG PRESENT has been entered.

8.2.2 ERROR MESSAGES

The majority of the following error messages relate to the controller so try changing this board first when an error message occurs.

GENERAL

-ERROR IN BUS TEST
-ERROR IN 8253 TEST
-ERROR IN CTC TEST
-ERROR IN BSC PROTOCOL
-ERROR IN SIO TEST IN SDLC PROTOCOL
-ERROR IN PLUG TEST IN SDLC PROTOCOL

TEST 1

-ERROR DATA-BUS
    .SIGNALS IOGON,EASTC,RWGOB

-ERROR SIO-BUS
    .SIGNALS SS1ON,IAD10-20,DB00-07
    .SIGNALS M100A,IORQB,RD00A,FZ8

-ERROR CTC-BUS
    .SIGNALS SCTCN,IAD10-20,DB00-07
    .SIGNALS MI00A,IORQB,RD00A

-ERROR 8253-BUS
    .SIGNALS S825N,IAD10-20,DB00-07
    .SIGNALS MI00A,IORDN,IOWRN,IORQB

TEST 2

-ERROR ON ALL CHANNELS
     .SIGNALS OSC12N,P1U40

-ERROR ON CHAN.0
     .SIGNAL OSC12N

-ERROR ON CHAN.1
     .SIGNALS OSC12N,ROOON

-ERROR ON CHAN.2
     .SIGNALS OSC12N,P1U40
     .SIGNALS OSC12N,ROOON

TEST 3

-SIGNAL ERROR IE0B1
.SIGNAL IE1OA TO PORT NSB2 FROM PORT NEB3
.SIGNALS IE1A1, IE1B1 FROM LDF9 BUFFER

-DAISY-CHAIN ERROR
.SIGNAL INCT1 FROM BISTABLE NO8
.SIGNALS INCTN and LATCH
.SIGNAL INTAN FROM NEV4

-NOT OCCURRED INT. OF CTC-CH.

-ERROR COUNTER CHAN.0 - FREQ.:
.VERIFY PATH FROM 8253-OUT2 TO CLK0-CTC

-ERROR COUNTER CHAN.2 - FREQ.:
.VERIFY PATH FROM 8253-OUT2 TO CLK2-CTC

-ERROR COUNTER CHAN.3 - FREQ.:
.VERIFY PATH FROM 8253-OUT1 TO CLK3-CTC

-ERROR COUNTER CHAN.1 - FREQ.:
.SIGNALS ICLK0,LODA0,SYXB0
.FF CHAIN DKL8,NFB3 PORT,NEB1 INV.

TEST 4

-CH. B TX UNDERRUN/END OF MESSAGE

-CH. B CRC/FRAMING ERROR NOT EXPECTED

-CH. B RECEIVE OVERRUN ERROR

-CH. B PARITY ERROR

-CH. A TX UNDERRUN/END OF MESSAGE

-CH. A CRC/FRAMING ERROR NOT EXPECTED

-CH. A RECEIVE OVERRUN ERROR

-CH. A PARITY ERROR

-CH. B DCD-ON INTERRUPT NOT OCCURRED
.DCD SIGNAL I0OON
.SIGNALS LOAD0,C000A,C0000,CKTAA

-CH. B SYNCHRONISM INTERRUPT NOT OCCURRED
.SIGNALS CKTA2,SA0ON,TXBA0,R0001,LOAD0

-CH. B END OF TRANSMISSION NOT VERIFIED
.SIGNALS CKTA2,SA0ON,TXBA0,R0001,LOAD0

```
-CH. B DCD-OFF INTERRUPT NOT OCCURRED
    .DCD SIGNAL I0OON
    .SIGNALS L0AD0,C000A,C0000,CKTAA

-CH. A SYNCHRONISM INTERRUPT NOT OCCURRED
    .SIGNALS RXDA0,SA001,CKTAA,A1030,L0AD0

-CH. A END OF TRANSMISSION NOT VERIFIED
    .SIGNALS RXDA0,SA001,CKTAA,A1030,L0AD0
```

TEST 5

```
-DCD-ON INTERRUPT NOT OCCURRED CH B
    .DCD SIGNAL I0OON';
    .SIGNALS I0OON,C000A,C0000,T0AD0

-SYNC-ON INTERRUPT NOT OCCURRED CH B
    .SIGNALS TXBA0,CKTA2,R0001,SA0ON
    .SIGNALS CNRYA,X24TT,ICLK0

-END OF TX NOT OCCURRED CH B
    .SIGNALS TXBA0,R0001,T0002

-DCD-OFF INTERRUPT NOT OCCURRED CH B
    .DCD SIGNAL I0OON

-STRING TRANSMISSION ERROR CH B

-SYNC-ON INTERRUPT NOT OCCURRED CH A
    .SIGNALS A1030,TXDA0,T0002,RXDA0
    .SIGNALS A1043,RXNRZ

-END OF TX NOT OCCURRED CH A
    .SIGNALS A1030,RXDA0

-STRING TRANSMISSION ERROR CH A

-ABORT/SEQUENCE ERROR CH B

-TX UNDERRUN ERROR CH B

-CRC ERROR CH B

-CTS INTERRUPT NOT EXPECTED CH B

-RX OVERRUN ERROR CH B

-DCD INTERRUPT NOT EXPECTED CH

-ABORT/SEQUENCE ERROR CH A

-TX UNDERRUN ERROR CH A
```

```
-CTS INTERRUPT NOT EXPECTED CH A

-CRC ERROR CH A

-RX OVERRUN ERROR CH A
```

TEST 6

```
-DCD-ON INTERRUPT NOT OCCURRED CH B
    .DCD SIGNAL I000N
    .SIGNALS I000N,X100N

-SYNC-ON INTERRUPT NOT OCCURRED CH B
    .SIGNALS TXBA0,CKTA2,R0001,SA00N
    .SIGNALS X24TT,XT000,XC00N

-END OF TX NOT OCCURRED CH B
    .SIGNALS TXBA0,R0002,XT000,XR000

-DCD-OFF INTERRUPT NOT OCCURRED CH B
    .DCD SIGNAL I000N

-STRING TRANSMISSION ERROR CH B

-SYNC-ON INTERRUPT NOT OCCURRED CH A
    .SIGNALS A1030,TXDA0,XC00N,RXDA0
    .SIGNALS A1043,RXNRZ,XR000

-END OF TX NOT OCCURRED CH A
    .SIGNALS A1030,RXDA0

-STRING TRANSMISSION ERROR CH A

-ABORT/SEQUENCE ERROR CH B

-TX UNDERRUN ERROR CH B

-CRC ERROR CH B

-CTS INTERRUPT NOT EXPECTED CH B

-RX OVERRUN ERROR CH B

-DCD INTERRUPT NOT EXPECTED CH.

-ABORT/SEQUENCE ERROR CH A

-TX UNDERRUN ERROR CH A

-CTS INTERRUPT NOT EXPECTED CH A

-CRC ERROR CH A

-RX OVERRUN ERROR CH A
```

8.3 LCUTT4: LCU TTL CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To check the operation of the line controller by simulating the transmission-reception operations.

HARDWARE REQUIRED

TTL line controller.

PRELIMINARY OPERATIONS

It is necessary to connect a loop plug on the controller or on the I/O cable as shown below:

ON CONTROLLER (I/O CONNECTOR)	ON CABLE (I/O CONNECTOR)
PIN A to PIN 1	PIN 2 to PIN 3
PIN B to PIN 2	PIN 4 to PIN 5
PIN C to PIN 3	PIN 6 to PIN 20
PIN D to PIN K to PIN 4	PIN 22 to PIN 23
PIN E to PIN F to PIN H	PIN 8 to PIN 18 to 25
PIN J to PIN 6	PIN 15 to PIN 17 to 24

LOADING PROCEDURE

Refer to section 1.3.2.

8.3.1 TEST DESCRIPTION

Refer to TEST DESCRIPTION for the GLAV2B program (section 8.1.1).

8.3.2 SERVICE AND ERROR MESSAGES

Service messages are indicated by a two digit hexadecimal code. Error messages have a four digit hexadecimal code; the last two digits indicate the error and the first two the associated service message. if an error occurs try changing the TTL line controller first.

- AA Board search
- AAAA Missing board or jumpers not connected properly
- 01 CTC interrupt test (CH0 -CH1)
- 0106 Daisy chain error - CTC interrupt not disabled
- 0107 Incorrect interrupts
- 02 CTC count test

- 0205 Wrong count of CTC, CH0 - CH1
- 03 Bus 8253 test
- 0301 Diagnostic clock not present - error on bus
- 04 CTC bust test
- 0402 Error on bus
- 05 8253 test
- 0504 wrong count of 8253
- 06 Asynchronous transmission test - OVERRUN and BREAK
- 0610 Error for the SIO overrun bit - break interrupts
- 0611 Error for reception interrupts
- 0612 Error for reception - transmission comparison
- 0613 Error for the SIO break bit
- 0614 Error on RXDA0 - TXDA0 - A142 or absence of same wires
- Asynchronous transmission test - parity error
- 070D Error of the SIO parity error bit
- 070E Error for reception - transmission interrupts
- 070F Error for reception - transmission comparison
- 08 Asynchrounous transmission test with even odd parity
- 080A Error for interrupt from external status of DCD-CTS
- 800B Error for transmission - reception comparison
- 800B Error for transmission - reception comparison
- 09 SIO bus test
- 0908 Error bus test
- 0A RTS, CTS, DCD loop test
- 0A09 internal loop between CTS-DCD not valid
- 0B SDLC transmission - hunt test
- 0B15 Error for the SIO hunt bit
- 0B16 Error for sync interrupt

- 0B17 Error for transmission - reception interrupt
- 0D SDLC transmission - address search test
- 0D19 Error for transmission - reception interrupt
- 0E SDLC transmission - abort transmission test
- 0E1A Error for transmission - reception interrupt
- 10 Monosync transmission - hunt test
- 101C Error for the SIO hunt bit
- 101D Error for sync interrupts
- 101E Error for transmission - reception interrupt
- 11 Bysinc transmission - hunt test
- 111F Error for hunt test
- 1120 Error for sync interrupts
- 1121 Error fortransmission - reception interrupts
- 13 SDLC test - external test
- 1323 Error for reception - transmission interrupts
- 1324 Incorrect interrupts on CTC, CH2 - CH3
- 1325 Loop A142 A not valid
- 15 RTS, CTC, DCD external loop test
- 1530 Loop CTC (on) - LODAO not valid
- 1531 Loop C141 - C142 not valid
- 1532 Loop C141 - C142 not valid
- 16 LINE NAME JUMPER TEST
- 1633 Error on line name jumpers
- 17 SDLC transmission - test NRZI
- 1734 Wrong operation of NRZI in transmission wrong reception of sync character
- 12 sync character transmission for PLL test
- 1222 Error for transmission - reception interrupts

8.4 LCUM04: MOIN5 TEST PROGRAM

PROGRAM PURPOSE

To check the operation of the line controller and the connection to MOIN5.

HARDWARE REQUIRED

TTL line controller MOIN5 board, cable of connection between line controller and MOIN5.

PRELIMINARY OPERATIONS

Check that the C03 dipswitch on the MOIN5 board is set as follows:

switch section 4 set to ON (logic level 1)
switch section 5 set to ON (logic level 1)
switch section 6 set to ON (logic level 1)
switch section 7 set to ON (logic level 1)
remainder sections set to OFF (logic level 0)

LOADING PROCEDURE

Refer to section 1.3.2.

8.4.1 TEST DESCRIPTION

Refer to the corresponding section 8.3.1 of the LCUTT4 program for the test description.

8.4.2 ERROR MESSAGES

The error messages are the same as described in program LCUTT4 section 8.3.2 with the exception of the external loop messages and the addition of the following messages. If an error occurs check the cable connection and then try changing the controller.

- 14 SDLC transmission with loop towards MOIN5.
- 1426 MOIN not present, loop 141-10 not valid.
- 1427 RTS Loop not valid.
- 1428 Error for transmission - reception interrupts.
- 1429 S10 synchronously not valid.

8.5 MOINV2: MODEM MOIN52 TEST PROGRAM

8.5.1 PROGRAM NAME: MOINV2

PROGRAM PURPOSE

The program is designed to check operation of the modem MOIN52 when used in connection with the G0300 or G0156 line controller.

HARDWARE REQUIRED

Video/keyboard controller, floppy disk unit, GLAV24 (G0300) or LCU242 (G0156) line controller, MOIN52 modem.

PRESETTINGS

The line controller and modem must be connected by a connection cable.

The two Dual line, 15-way, 100 mm connectors must be connected as shown below:

V24 PLUG		MOIN52 PLUG
PIN 1	to	PIN N
PIN 2	to	PIN M
PIN 3	to	PIN L
PIN 4	to	PIN R
PIN A	to	PIN 7
PIN B	to	PIN 8
PIN C	to	PIN 9
PIN D	to	PIN 10
PIN F	to	PIN 11
PIN H	to	PIN 12
PIN J	to	PIN J
PIN L	to	PIN 14
		PIN 13 to PIN 5
		PIN P to PIN S

NOTE

The operator must remove any existing connections between the G0300 (or G0156) and MOIN52 boards and fit the appropriate cable.

LOADING PROCEDURE

Refer to section 1.3.2.

8.5.2 TEST DESCRIPTION

The M01N52 controller consists of analog circuits, therefore, individual components cannot be tested.

The modem characteristics are set using the four DIP-switches on the PCB.

As the M01N52 external test is performed with a very short connector loop, the modem features relating to line characteristics (impedence, attenuation, noise etc.) cannot be checked.

Some of the DIP-switch settings not considered in the controller test are listed below:

a) Line impedence selection (600, 150 Ohm)

b) Connection selection (point-to-point, multi-point)

c) Transmision level selection (0 db, +6 db)

d) Receive equalization selection

e) Modulation type selection (non-differential, differential on 1, differential on 0)

f) Transmission pre-distortion selection.

g) Operating velocity selection (1,200, 19,200 baud)

h) Delay between RTS and CTS selection.

The following types of pre-setting are taken into consideration:

a) Transmission filter setting

b) Signal C105 type selection (fixed/varying)

c) Signal C108 type selection (fixed/varying)

d) Interface type enabling (V24/TTL)

e) Operation type selection (2-wire/4-wire, half-duplex/full duplex)

f) Continuous carrier transmission selection.

The DIP-switch setting is not detected by the diagnostic program as the DIP-switches cannot be read by program.

Settings can only be considered not significant for program execution when no defects affecting modem operation arise after a change in the setting.

Receive pre-distortion selection, for example, does not affect modem characteristics in the test, since selection of this feature cannot be detected at test level as the modem has no send/receive lines. Note: Changing this setting involves addressing two different PROM pages so that, if one were incorrectly programmed, circuit operation could be impaired.

The tests carried out are:

- MOIN INTERNAL LOOP BACK TEST 1
- MOIN EXTERNAL LOOP BACK TEST 2.

1. The first test checks out the MOIN using the board internal loop (and thus bypassing the line transformers).

2. The second test is similar to the first test except that, the external loop is used for the tests and in this way the line transformers are also tested.

8.5.3 ERROR MESSAGES

If an error occurs first check the connection to the modem and the presettings if this is unsuccessful try changing the controller board before the modem.

There are two types of error message:

- for blocking errors
- for non-blocking errors

Messages associated with blocking errors are:

- ERROR IN DATA TRANSMISSION

  This may, in some cases, be accompanied by an additional message:

  "VERIFY LINE TRANSFORMERS"

- SYNCHRONIZATION ERROR

  indicating that the receiver and transmitter cannot be put in sync. Again, an additional message may be provided:

  "VERIFY SYNCHRONIZATION CIRCUITS"

- V24 CONTROLLER ERROR

  indicating some form of error on the board driving the MOIN.

Messages associated with non-blocking errors are:

- CLEAR TO SEND-ON NOT VERIFIED
- CLEAR TO SEND-OFF NOT VERIFIED
- DATA CARRIER DETECTED-ON NOT VERIFIED
- DATA CARRIER DETECTED-OFF NOT VERIFIED

  These messages refer to transitions of signals DCD (C109) and CTS (C106).

  They may be accompanied by the following additional messages:

- "DCD DIGNAL C109"
- "CTS SIGNAL C106"
- "VERIFY RTS-CTS DELAY CIRCUITS"
- "VERIFY DLD HYSTERESIS AND DLD CIRCUITS"
- "VERIFY MODUL. AND DEMODUL. CIRCUITS"

  Other non-blocking error messages are:

- ERROR IN CALLING INDICATOR TEST

  followed by the message:

  "SIGNAL A125A"

  when signal A125A is found to be at logic level "0"

- ERROR: MODEM ALREADY CONNECTED

  followed by the message:

  SIGNAL C107

  when the modem is found to be connected before the connection command is given.

- ERROR IN MODEM TO CONNECT TO LINE

  followed by the additional message:

  "SIGNAL C107 AND C105"

  when the modem cannot be connected to the line.

- ERROR: MODEM NOT CONNECTED TO LINE

  indicating that the modem, which should be connected to the line through a hardware pre-setting, is not connected.

- ERROR: MODEM ALREADY IN DIAGNOSTIC LOOP

  followed by the additional message:

  "SIGNAL C142"

  indicating that the modem is in diagnostic loop before the command setting it in loop is issued.

- ERROR: DIAGNOSTIC LOOP NOT ACTIVE

  followed by the additional message:

  "SIGNALS C142 AND C141"

  when the modem cannot be set for diagnostic operation.

8.6 TWIN05: TWIN CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

This program is designed to check operation of the fast and slow TWIN line controllers.

HARDWARE REQUIRED

The asynchronous TWIN controller "GLATW" boards G0327 and G0151.

PRESETTINGS

If the whole program is to be carried out, two plugs are required, one for the current loop, the other for the V24 loop.
The plug pin connections are as shown below:

	CURRENT LOOP PLUG				V24 PLUG			
PINS TO BE CONNECTED:	1-A	2-B	3-C	4-D	1-A	2-B	3-C	4-D
	5-E	6-F	5-6	E-F	5-E	6-F	7-H	8-J
	8-H	H-J	9-K	11-M	9-K	10-L		
	13-N	N-P	14-R					

LOADING PROCEDURE

Refer to section 1.3.2.

8.6.1 TEST DESCRIPTION

1) BUS TEST

This test checks the data bus and the controller.

Data represented XX varies in relation to jumper settings and provides information should a malfunction occur.

Depending on the controller, the following data is displayed:

- Controller G0327

```
DRIVER NAME        ADDRESS %E7 :  CF
STATUS REGISTER    ADDRESS %A1 :  XX
CH.A INFORMATION AND DIPSWITCHS FOR
DRIVER G0327:(BIT 0-4)BOARD POS.A10
                   ADDRESS %E3 :  XX
CH.B INFORMATION AND DIPSWITCHS FOR
DRIVER G0327:(BIT 5-7)BOARD POS.A10
      AND(BIT 0-1)BOARD POS. A09.5.
                   ADDRESS %E5 :  XX
```

- Controller G0151

```
DRIVER NAME       ADDRESS %E7 :  CF
STATUS REGISTER   ADDRESS %A1 :  XX
CH.A INFORMATION AND DIPSWITCHS FOR
DRIVER G0151:(BIT 1-3)BOARD POS.D09
      AND(BIT 0-1)BOARD POS.D09. L.
                  ADDRESS %E3 :  XX
CH.B INFORMATION AND DIPSWITCHS FOR
DRIVER G0151:(BIT 1-3)BOARD POS.E09
      AND(BIT 0-1)BOARD POS. E09.L.
                  ADDRESS %E5 :  XX
```

2) 8253 TEST

Channels 1 and 2 of the 8253 counter-timer are checked. Only error messages are displayed.

3) DART 1

The SIO-DART is tested using the internal loop:
a string of characters is transmitted and then using the internal loop received. A comparison is then made with the data transmitted and the data received.

4) DART 2

This test is similar to the DART 1 test except that the external loop is used. The test is only carried out if the operator has stated that the external plug is in position.

If the operator during the preprogramming stage has entered that the plug is not in place and the test is run with the plug connected, then the following message is displayed:

```
EXTERNAL PLUG IS DECLARED ABSENT !!
         REQUEST   PARAMETER
                     RANGE   DEF VALUE
HAVE YOU INSERTED NOW?Y=1/N=0  1 =
```

After inserting the plug the operator is requested to comfirm that the plug is place otherwise the program terminates.

8.6.2 ERROR MESSAGES

Error messages displayed in the course of the program depend on the diagnostic level chosen by the operator.

At "diaglev" 1 (the basic level), only an indication of the fault and the major component involved is given; at diaglev 2, in addition to the diaglev 1 information, a list of the signals associated with the fault is is also given.

An example of both forms of message is given below:

diaglev = 1

error message:

8253=BUS ERROR

diaglev = 2

previous message plus the following information:

```
SIGNALS: S8253;1AD10/1AD20;IORDN=  I053N
         IORWRN=  WRITE,IORQB;
```

At diaglev 2, the history of the error is printed out and the test can be continued by entering "5".

8.7 TW1005: LCU TWIN RS422 CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To check that the line controller is functioning correctly by testing the olibus interface, the CPU, the ROM, the RAM and the management of the two serial channels.

HARDWARE REQUIRED

LCU TWIN 422 line controller (G0236).

PRELIMINARY WARNING

Before running the test, the operator must disconnect any external devices connected and fit the loop plug to the board, when required.

SETTINGS:

If the test is run with external loop, a plug is needed to produce the hardware loop on the terminal strip. The pin connections are shown below:

PIN 5 to PIN 26
PIN 6 to PIN 25
PIN 9 to PIN 22
PIN 10 to PIN 21

LOADING PROCEDURE

Refer to section 1.3.2.

8.7.1 TEST DESCRIPTION

MEMORY INITIALIZATION TEST

This test examines the basic operation of the controller, by checking first RAM initialization and then the controller busy status.

MEMORY (HOST) TEST

Checks operation of the dual-port memory as host. The test is in three separate parts:

Z8002 TEST

The Z8002 microprocessor is verified by checking the instructions involving internal operations.

MEMORY TEST (SLAVE)

A check on the internal operation of the dual-port memory and bus drivers. The tests are the same as in the host memory test.

ROM TEST

The ROM controller is tested. The CRC is taken and compared with the value stored in the ROM. When no errors are found, the next test is run.

INTERRUPT TEST

The interrupt vector load operations are checked; this test also ensures that the controller being tested is the only source of interrupt.

Z-CIO (TIMERS)

The timers are checked in their three possible modes of operation: pulse output, one shot output and square wave output. Where possible, the timers are cascade-connected.

Z-CIO (PARALLEL I/O)

The Z-CIO parallel ports are checked by performing a number of write operations followed by read operations to ensure that the individual line handling signals are correct.

LINE DRIVERS TEST (CHANNEL B)

A check on the line drivers and their circuits. The baud rate generator and all possible line signal paths are tested.

Z-SCC TEST (CHANNEL A/B)

The LSI Z-SCC component and the logic of the related lines are tested by checking that the reception/transmission channels function correctly.

INTERNAL INTERRUPT TEST

The controller internal daisy chain is tested by checking that all devices in the daisy chain are enabled correctly using the interrupt logic.

TX/RX LOCAL LOOP TEST (CHANNEL B)

A reception/transmission test is run simultaneously on both channels at a higher speed than normal.

8.7.2 ERROR MESSAGES

The programs provides the following error messages which can be displayed as a single message or a number of messages as a result of specific tests.

SYSTEM DISABLING MESSAGES

- *** PRIVILEGE INSTRUCTION TRAP *** = execution in user mode of a privilege instruction.
- *** SEGMENT TRAP = access of memory area not managed by the MMU
- *** ILLEGAL MEMORY TRANSACTION *** = accesss of memory area not present.
- LCU ..... = parameters provided by Pascal sub-system modules out of tolerance.

DIAGNOSTIC MESSAGES

- ERROR ON MEMORY INITIALISATION = error on initialization of the RAM by the controller.
  VERIFY THE ADDRESS LINE NUMBER (XX) ....(YY)
- ERROR ON ODD BLOCK = error on the odd address ROM chip.
- ERROR ON EVEN BLOCK = error on the even address ROM chip.
- ERROR ON ALL BLOCKS = error on both ROM chips.
- TEST NOT FINISHED = possible faults on the RAM slave chips in addition to those already signalled.
- ERROR ON CHIP 1 (LOW AND ODD) = error on chip for the odd byte and RAM low address area.
- ERROR ON CHIP 2 (LOW AND EVEN) = error on the chip for the even byte and RAM low address area.
- ERROR ON CHIP 3 (HIGH AND ODD) = error on the chip for the odd byte and RAM high address area.
- ERROR ON CHIP 4 (HIGH AND EVEN) = error on the chip for the even byte and RAM high address. area.
- CPU TEST ERROR = incorrect instruction execution of the CPU Z8002 .
- NOT INTERRUPT = controller not interrupting the system CPU.
- BAD INTERRUPT VECTOR = interrupt vector incorrect.
- FAILURE ON PARALLEL I/O = fault on the parallel ports of the chips specified by the following error message.

- Z-CIO 1 = Z-CIO 8036 dedicated to channel A.
- Z-CIO 2 = Z-CIO 8036 dedicated to channel B.
- Z-CIO 1 & 2 = both Z-CIO 8036s.
- Z-CIO 1 TIMER N.X = fault in timer no. X, dedicated to channel A.
- Z-CIO 2 TIMER N.X = fault in timer no. X, dedicated to channel B.
- BAD CLOCK OR ERROR ON COUNTING = error on counter or controller clock.
- ERROR ON RECEIVED BLOCK = error on data received.
- RX NOT READY = receiver still not ready after time-out has elapsed.
- TX NOT READY = transmitter not ready after time-out has elapsed.
- INTERNAL LSI LOOP = with an internal Z-SCC loop.
- ON BOARD LOOP = with a controller internal loop.
- EXTERNAL LOOP = with an external loop (plug).
- *** CHANNEL "A" *** = the diagnostic messages which follow refer to channel A.
- *** CHANNEL "B" *** = the diagnostic messages which follow refer to channel B.
- BAUD RATE GENERATOR = baud rate fault in specified channel.
- UNDEFINABLE FAILURE = interrupt received, other than the one expected during the interrupt test.
- FAILURE ON INTERNAL INTERRUPT = interrupt mechanism fault: message following specifies the component.
- FAILURE ON INTERNAL DAILY CHAIN = internal daisy chain fault: message following specifies the component.
- Z-SCC = the faults described above can be attributed to the Z-SCC 8030.
- INTERFACE SIGNAL FAILURE = malfunctions in certain signal pairs, listed below:
  - 103/107 = data tx/DSR
  - 111/125 = rate selector/ring indicator
  - 141/142 = local loop back/test indicator
  - 105/106 = RTS/CTS
  - 108/109 = DTR/DCD

- FAILURE ON DIAGNOSTIC LOOP = errors due to tests on the above signals with loop connected on the controller.

- ERROR NUMBER (X) = malfunction on one or more logic chains, obtained by using the internal "on board" loop plug (x is a number between 1 to 7).

- TRANSMITTER TIME OUT = time-out in transmission.

- RECEIVED TIME-OUT = time-out in reception.

- RX PARITY EERÖR = parity error in data received.

- RX OVERRUN ERROR = one or more characters lost in reception.

- RX FRAMING ERROR = SDLC protocol error.

- RX DATA ERROR = error in data block received.

- RX BUFFER OVERFLOW = more characters received than expected.

- RX BUFFER FULL = more characters received than transmitted.

- UNKNOWN INTERRUPT = an interrupt served on an unprogrammed vector or an unexpected interrupt.

- WITHOUT ALL LOOPS = the diagnostic messages which follow have been produced from tests not using the internal or external loop.

- WITH INTERNAL LOOP = the diagnostic messages which follow have been produced from tests using the internal loop.

- WITH CROSSING LOOP = the diagnostic messages which follow have been produced from tests with external loop selected without verifying if the loop is present.

- FAILURE ON DATA = data signal fault; the Z-SCC and associated components should be checked.

- FAILURE ON CLOCK = data signal fault; the Z-SCC and associated components

8.8 LIONV4: LION 9.6 CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To check the line controller operation.

HARDWARE REQUIRED

LION 9.6 Kbaud line controller (GO333) (master and slave or slave only).

LOADING PROCEDURE

Refer to section 1.3.2.

8.8.1 TEST DESCRIPTION

8253 TEST

This test is carried out on all three channels of the 8253 timer and consists of loading the internal decrementing counter with a certain value and at a given interval making a comparison with a value set in a register.

CTC TEST

Tests are carried out on channels 0, 1, 3 of the CTC. Channel 0 is tested as in a counter, channel 1 is tested as a timer and channel 3 is also tested as a counter.

SIO-BSC TEST

The test consists of an exchange of 128 characters on channel A of the SIO with a 7 bit + a parity bit separation between each stream of characters.

SIO- SDLC TEST

The test consists of an exchange of 256 characters on channel A of the SIO with a 8 bit separation between each stream of characters.

LINE-BSC

This test initially transmits 128 characters using BSC protocol from the master controller to the slave, and then from the slave to the master. At the end of the transmission a comparison is made, byte for byte of the data in the two buffers TX and RX . A test is made of the data transmitted and the data received.

LINE- SDLC LINE

This test initially transmits 256 characters using SDLC protocol from the master controller to the slave, and then from the slave to the master. At the end of the transmission a comparison is made, byte for byte of the data in the two buffers TX and RX.

CRC TEST

The CRC test produces two different polynomials one from the master and one the slave which are used to provoke a CRC error. If a CRC error has not been detected the system flags a fault, otherwise the CRC error is cancelled.

8.8.2 ERROR MESSAGES

If an error occurs and there is more than one controller try changing the master controller first and then any slaves before checking the CPU.

- 8253 ERROR (LBTA)
- ERROR 8253 CH. 0/2/3
- Z80 CTC ERROR (LBTO IN D8)
- ERROR CTC CH. 1/2/3
- INTERNAL/LINE DCD-ON/OFF INTERRUPT NOT OCCURRED
- INTERNAL/LINE CTS-ON/OFF INTERRUPT NOT OCCURRED
- INTERNAL/LINE SYNCR-ON INTERRUPT NOT OCCURRED
- INTERNAL/LINE CRC-ERROR
- INTERNAL/LINE RX/TX OVERRRUN/UNDERRUN
- INTERNAL/LINE PARITY ERROR INTERRUPT
- INTERNAL/LINE CH.B UNEXPECTED INTERRUPT
- INTERNAL STRING-TRANSMISSION ERROR
- INTERNAL/LINE END OF TRANSMISSION NOT OCCURRED
- INTERNAL TX-UNDERRUN INTERRUPT NOT OCCURRED
- INTERNAL/LINE ABORT/SEQUENCE RECEIVE
- INTERNAL FRAME-CRC ERROR
- TX/RX-INTERRUPT ON SIO-RX/TX
- CRC-TEST SDLC FREQ.=
- ERROR ON CRC CHECK (TESTED-SIO RX/TX CH.)
- DIFFRERENCE BETWEEN TX-BUF. AND RX-BUF.

8.9 96ERM6: LION 9.6 (MASTER) ERROR RATE PROGRAM

PROGRAM PURPOSE

To evaluate the error rate in exchanges of messages between a master and a number of slaves interconnected by a LION local line.

HARDWARE REQUIRED

Line controllers linked by a LION network.

The 96ERS6 program must be run on each of the declared slave workstations before loading the 96ERM6 (master) program on the master workstation. New slave workstations can be added, substituted or disconnected from the lion network by hitting the ENTER key on the workstation as indicated in the text. The 96ERS5 program must then run on each of the new workstations before continuing with the master program.

NOTE:

The MASTER and SLAVE polling name must not be FF.

LOADING PROCEDURE

Refer to section 1.3.2.

8.9.1 TEST DESCRIPTION

SYNCHRONISATION MESSAGES

The synchronisation messages contain the inherent parameter data which must be passed on to each slave before starting the tests.

Each slave in turn tests the synchronisation message and retransmits a similar message to the master. The master then checks the message received and if there is an error retransmits the original message. After repeating this procedure three times, if the error persists, the slave responsible for the error is excluded from the remaining tests and the message "slave XX not read" is displayed, where XX is the slave's polling name.

After testing each slave the program exits the synchronisation phase and enters the crc phase.

CRC TEST MESSAGES

The Cycle Redundancy Check (CRC) comprises generating and checking 20 test bytes on the master and on each slave.

In case of error on a slave the message "crc gen/check slave XX" is generated, where XX is the slaves polling name. Similary if an error is found on the master the message "crc gen/check error" is displayed.

After completing the crc tests the program starts the transmission of the test messages.

TEST MESSAGES

The test message comprises 14 control bytes followed by up to 32 blocks each of 32 bytes.

CHANGE TEST MESSAGE

At the end of the transmission and reception of the test block(s) to each slave and the subsequent tests, the master sends a change test message which causes a change in the baud rate of any subsequent test transmission.

8.9.2 ERROR MESSAGES

If a blocking error occurs re-load the program and/or change controller.

- SLAVE XX NOT READY
- MASTER WRONG, PLEASE RUN LION 9.6 TEST PROGRAM
- MASTER SENDS ON LINE TO ALL THE SLAVES CONNECTED
- END OF TRANSMISSION/SYNCHRONIZATION NOT OCCURRED
- RECEIVER SYNCHRONIZATION NOT OCCURRED
- UNOCCURRED RECEPTION FROM SLAVE XX OR ABORT INTERUPT
- END OF SYNCHRONIZATION NOT OCCURRED
- DCD DOWN INTERRUPT NOT OCCURRED
- ERROR IN FRAME
- UNKNOWN NUMBER OF ERRORS IN TRANSMISSION TO SLAVE XX
- UNEXPECTED FRAME FROM SLAVE XX
- FRAME FROM UNKNOWN SLAVE
- XXXXXXX ERRORS YYYYYYY BIT EXCHANGED
- CRC GEN/CHECK ERROR SLAVE XX
-

```
**************************
XXXXX BAUD RATE SLAVE YY
ZZZZZZ BIT EXCHANGED
WWW/KK ERRORS IN TRANSMISSION/RECEPTION
JJJJJJ TOTAL ERRORS DETECTED
**************************
```

8.10 96ERS6: LION 9.6 CONTROLLER (SLAVE) ERROR RATE PROGRAM

PROGRAM PURPOSE

To load the 96ERS6 program and enter the preprogram parameters on each slave controller connected by a lion network, in order to evaluate the error rate in exchanges of messages between the slave(s) and master controller.

HARDWARE REQUIRED

Line controllers connected by a LION local network.

NOTE:

After loading the program and entering the preprogram parameters as described in this section reference should be made to the chapter on the MASTER ERROR RATE PROGRAM for the continuation of the test description.

LOADING PROCEDURE

Refer to section 1.3.2.

8.10.1 TEST DESCRIPTION

Each slave is loaded in turn with the 96ERS6 program which specifically requires the polling number and slot number of each slave to be entered in the preprogramming stages. The master controller then takes over control and transmits test messages to each slave as described in the chapter on the MASTER ERROR RATE PROGRAM. The slaves are then required in turn to transmit a similar message to the master controller for examination and evaluation.

8.10.2 ERROR MESSAGES

The following messages are available on the slave workstations (re-run program and/or change controller board if there is a blocking error):

- UNOCCURRED PROGRAM START
- XXXXXXXX ERRORS DETECTED YYYYYYYY BIT
- UNRECOGNISED MESSAGE
- MESSAGE LENGTH UNKNOWN
- UNKNOWN TYPE OF TEST
- ERROR IN FRAME TRANSMISSION
- SLAVE WRONG; PLEASE RUN LION 9.6 TEST PROGRAM
- SYNCHRONIZATION UNOCCURRED

- END OF TRANSMISSION/SYNCHRONISATION NOT OCCURRED

- RECEPTION START UNOCCURRED

- ABORT INTERRUPT NOT OCCURRED

- DCD OFF INTERRUPT NOT OCCURRED

- UNKNOWN NUMBER OF PATTERN

- Z80 SIO TRANSMIT UNDERRUN INTERRUPT

- ```
  ****************************
  XXXXX BAUD SLAVE YY
  WWWWW BIT RECEIVED
  KKKKK ERRORS DETECTED
  ****************************
  ```
  ```

8.11 STARLO: STARLAN-DUMB ERROR RATE TEST PROGRAM

PROGRAM PURPOSE

The program checks the operation of a number of controllers on a STARLINE-DUMB line system and determines the error rate of the system.

HARDWARE REQUIRED

Starlan-dumb line controllers (GO431, 128 max) and a STARLAN-DUMB line.

HARDWARE SETTINGS

The controller is connected to the C-BOX by a drop cable; the C-BOX is then connected to the Hub (distribution junction).

N.B.

The controllers under test are connected to the network via telephone lines; these controllers (each in an NLS3000 or NLS8000 system) regulate access to the network and are known as stations. The number of stations (or NODES) that can be connected is directly related to the system memory available to record and store error statistics on the control station. In this program, the number of stations has been limited to 128.

CAUTION
In this program a station is used as the MASTER or CONTROL_NODE whilst the other stations are treated as SLAVE NODES. It is necessary to run the program on the slave stations and then on the master station.

LOADING PROCEDURES

Refer to section 1.2.3.

8.11.1 TEST DESCRIPTION

TEST 1 - LCC LOOPBACK TEST

The Local Communication Controller (LCC) is set in internal loop mode and a data package of 1518 bytes is transmitted via the internal loop. A comparison is then made of the data transmitted with the data received. If the operation is successful the LCC is set in external loop mode and a similar test is carried out on the controller external loop using a data package of 18 bytes.

TEST 2 - HUB LOOPBACK TEST

This test is similar to the external loop test of TEST 1 except that 18 byte data package is routed via the HUB connection of the STARLAN LINE.

The results are observed, the LCC taken out of loop mode and the test terminated. For the purposes of this test, there should be no traffic on the cable.

TEST 3 - PHYSICAL LINK TEST

This test looks for open or short circuit on the telephone cable by transmitting a test signal and measuring the time taken for the signal to return. There should be no other signals (or data traffic) on the cable.

TEST 4 - NO CHANNEL CONTENTION ERROR RATE

The CONTROL station polls each station it finds on the network and makes up a list of stations which have acknowledged its call or follows a list selected by the operator and deletes from the list any station which does not acknowledge.

The CONTROL station then transmits a series of data packages, in turn to the stations on its list. Each slave station in turn checks the data package it receives, signals any errors it finds on its console, updates its records and sends the package back to the CONTROL station, with details of any reception errors.

The CONTROL station then evaluates the error rate of the section of the line connected to each SLAVE station and displays the results.

N.B. There should be NO contention for the channel under test by any other controller during transmission.

The operator can, during the test, add or delete a station from the test list by calling up the CONTROL NODE COMMAND MODE using the SKIP key and modifying the NODE list.

TEST 5 - CHANNEL CONTENTION ERROR RATE

This test determins the error rate of a network when a channel is being contended by other stations and when there are data collisions. The CONTROL station sends a data package to all the stations in the network, and requests all receivers to send back the data package.

The data received is then checked and an error rate table displayed. **N.B.** Traffic is one way towards the CONTROL NODE. If there are a number of CONTROL NODES i.e. NODE groups on the same network, then the nodes communicate only with their own CONTROL NODE.

TEST 6 - CROSS TRAFFIC ERROR RATE

This test determines the cross traffic error rate, as in true network operations. The network is set up so that each node is able to communicate with all the other nodes in the network or with subsets of nodes.

The CONTROL station informs all stations connected to the network of the start of the test and of the end of the test when it finds no more traffic on the network for a specific period. The statistical error rate is then updated for each node.

8.11.2 SERVICE, ERROR AND SUMMARY MESSAGES

SERVICE MESSAGES

- **CONNECTION PHASE...** = Start of node connection verification phase.

- **...END CONNECTION PHASE** = End of connection phase.

- **POLLING PHASE...** = Start of polling phase, or error rate without channel contention test (test 4). This message is issued at the end of the connection verification phase, and only if at least one connection has been successful.

- **...END POLLING PHASE** = End of the polling test.

- **0 CONTROLLER INITIALIZATION** = Start of Starlan controller initialization phase.

- **CONTROL NODE COMMAND MODE** = This message is issued when the operator wishes to modify the list of nodes during the polling test, by using the "SKIP" key.

  NODE xxx DISCONNECTED/CONNECTED

- **CONTENTION PHASE...** = Start of error rate with channel contention phase (test 5).

- **...END CONTENTION PHASE** = End of test 5.

- **CROSS TRAFFIC PHASE...** = Start of error rate with cross traffic phase (test 6).

- **...END CROSS TRAFFIC PHASE** = End of test 6.

- **TX PACK.NR. xxxxxx TO NODE yyy** = Indicates that a packet has been sent to node yyy.

- **RX PACK.NR. xxxxxx FROM NODE yyy** = Indicates that a packet has been received from node yyy.

- **TX PACK.NR. xxxxxx TO C_NODE** = Indicates on the node console that a packet has been sent to the control node.

- **RX PACK.NR. xxxxxx FROM C_NODE** = Indicates on the node console that a packet has been received from the control node.

- **CONTROLLER BOARD RESET** = Start of controller reset phase.

- **LCC INITIALIZATION/SOFTWARE RESET/CONFIGURATION** = Refers to the initialization/software reset/configuration phase of the Local Communication Controller (LCC 82586) phases.

- **INDIVIDUAL ADDRESS SET-UP** = Start of individual node address set-up phase.

- **LCC DIAGNOSIS** = Start of LCC autodiagnostic phase.

- **RU START** = Start of 82586 Receive Unit (RU) receive phase.

- **CONNECTION CODE RECEIVED** = Indicates on the node console that a packet containing the polling test connection code has been received from the control node.

- **CONNECTION ACKNOWLEDGE TRANSMITTED** = Indicates on the node console that a connection acknowledge packet has been sent to the control node.

- **DISCONNECTION CODE RECEIVED** = Indicates that a packet containing a disconnection code has been received. On receiving such a code, the node program automatically disconnects.

- **xxx NODE(S) STILL CONNECTED** = Indicates at the end of the polling test how many nodes are still connected in the network.

- **NO LINK PROBLEM IDENTIFIED** = Indicates that the reflectometric (TDR) test has completed successfully.

- **FAIL DISTANCE (IN CLOCK CYCLES) IS xxx** = Indicates the distance (expressed in clock cycles) between the node from which the TDR TEST was activated and the error.
  This distance can be calculated in metres as follows:

$$DISTANCE = (TIME * Vs / 2) * Fs$$

where:
TIME --> Value of the distance in clock cycles
Vs --> Transmission speed of the wave on the cable (M/s)
Fs --> Frequency of serial clock

The accuracy of this measurement is +/- (Vs / 2)*Fs.

- **INTERNAL LOOPBACK TEST PASSED** = Indicates that the LCC internal loopback test has been completed successfully.

- **HUB LOOPBACK TEST PASSED** = Indicates that the HUB loopback test has been completed successfully.

ERROR MESSAGES

Unless otherwise indicated change controller if there is a blocking error.

- **NODE xxx NOT CONNECTED** = Indicates to the operator that node xxx, which was to be inserted in the list, does not respond with confirmation of connection.

- **xxx: NO SUCH NODE** = Indicates that node xxx, which was to be deleted from the list, was not present in the list.

- **LIST FULL/EMPTY** = Indicates that the list of nodes is full, and thus no further nodes can be inserted or empty thus no nodes can be deleted.

- **xxx: NODE ALREADY EXISTS** = Indicates that node xxx, which was to be inserted in the list, is already in the list.

- **NO CONNECTION POSSIBLE** = This message is issued at the end of the polling test connection phase (TEST 4), if no node responds with confirmation of connection.

- **UNKNOWN ERROR CODE** = The purpose of this message is to protect the program from any firmware problems, and is issued if an I/O routine returns an unknown error code.

- **HUB CABLE PROBLEM IDENTIFIED** = Indicates a problem in the Hub cable.

- **OPEN/SHORT ON THE LINK IDENTIFIED** = Indicates an open/short circuit on the telephone cable.

- **EXCCESSIVE COLLISION TRANSMISSION FAILURE** = Indicates an interruption in an attempt to send, as the number of collisions already verified exceeds the maximum allowed amount.

- **NO CARRIER SENSE SIGNAL DURING TRANSM.** = Indicates that the Carrier Sense signal was not detected during transmission.

- **CRC ERROR** = Indicates a CRC error on the packet received.

- **ALIGNMENT ERROR** = Indicates an alignment error on the packet received.

- **RU RAN OUT OF MEMORY** = Indicates that the receive unit (RU) did not have enough memory available to store the incoming packet.

- **PACKET TOO SHORT** = Indicates that the packet received had fewer bits than the minimum packet length configured in the controller initialization phase.

- **HARDWARE ERROR** = This message is issued when there is an error attributed to the controller HW.

- **DUAL PORT MEMORY UNAVAILABLE** = Indicates that the program cannot effect read and write operations in Dual Port Memory.

- **RX TIMEOUT** = Indicates that the maximum time allowed in the polling test for receiving the response packet from the polled node has expired.

- **UNKNOWN PACKET TYPE** = Indicates that in the "PACKET CODE" field of the frame received there is an unexpected code in part of the test.

- **HUB TEST FAILURE** = Indicates that an Hub fault was detected during the frame transmission phase.

- **TIMEOUT ON COMMAND EXECUTION** = Indicates that the maximum time allowed for the execution of a command by the LCC has expired.

- **INIT FAILURE. UNAVAILABLE MEMORY** = Indicates that during the Dual Port memory frame initialization phase, an error occurred due to insufficient memory to allocate the identifiers.

- **LCC RESET NOT ACCEPTED** = Indicates that due to some problem the LCC has not accepted the software reset command.

- **IA SETUP COMMAND NOT ACCEPTED/EXECUTED** = Indicates that the LCC has not accepted/executed the individual node address set-up command.

- **START RX NOT EXECUTED** = Indicates that the frame receive enable command has been interrupted due to an LCC problem.

- **CONFIGURE COMMAND ABORTED/NOT ACCEPTED** = Indicates that the LCC has not aborted/not accepted the configure command.

- **TDR COMMAND NOT ACCAPTED** = Indicates that due to a problem the LCC has not accepted the TDR command (open/short circuit on the telephone cable).

- **DIAGNOSE COMMAND NOT EXECUTED** = Indicates that the autodiagnostic command has been interrupted due to an LCC problem.

- **LCC FAIL** = Indicates that an error attributed to the LCC has been detected.

- **INTERNAL LOOPBACK TEST FAILED** = Indicates that the LCC internal loopback test has failed.

- **HUB LOOPBACK TEST FAILED** = Indicates that the Hub loopback test has failed.

- **NMI TIMEOUT DURING BOARD RESET** = Indicates that during the controller reset phase the NMI was not generated by the CPU within the maximum allowed time.

- **MORE THAN ONE NODE HAS THE LOGNAME xxx** = This message warns the operator that more than one node responded when node xxx was polled in the connection verification phase of the polling test.

- **PACKET FROM UNKNOWN C NODE RECEIVED** = Indicates on the node console that a packet has been received from a different control node than the one selected.

- **PACKET FROM WRONG NODE RECEIVED** = Indicates in the polling test on the control node console that a packet was received from a different node than the one polled.

- **MORE THAN ONE PACKET IN RECEIVE AREA** = Indicates during the polling test on the control node console that more than one packet was received after a node was polled.

SUMMARY MESSAGES

At the end of the test, a summary of the statistics obtained is displayed. The type of station (NODE or CONTROL NODE) together with results of tests on each station are displayed as follows:

```
TEST TYPE                 y      y = test type
NODE NUMBER               n      n = NODE logic name
CONTROL NODE NUMBER       nn     nn = CONTROL NODE logic name
- TX PACKETS              xx
- DEFERENCES              xx     xx = numbers
- TOTAL COLLISIONS        xx
- RX PACKETS              xx

- BAD RX  PACKETS         xx
- CRC ERRORS              xx
- ALIGNMENT ERRORS        xx
- OUT MEMORY RESOURCES    xx
- DMA OVERRUN ERRORS      xx
- MINIMUM LENGTH ERRORS   xx

- NODE BAD RX PACKETS     xx
- CRC ERRORS              xx
- ALIGNMENT ERRORS        xx
- OUT MEMORY RESOURCES    xx
- DMA OVERRUN ERRORS      xx
- MINIMUM LENGTH ERRORS   xx
```

NOTES: The first part of the table refers to transmission/reception to the individual NODE stations. In test 4, the number of receptions is the total number of packages received by the node (correct and incorrect) while in the other tests, it is only the correct number of packages received.

Error rate data given in the second part of the table refers to the node indicated in test 4, but in test 5 and 6, it represents the sum total of errors found on all packages received and is accompanied, in these cases, by the heading "ERRORS ON ALL RECEIVED PACK. DURING TEST".

The third part of the table refers to the results test 4 node error rate.sponding to

8.12 SLANC2: STARLAN-DUMB CONTROLLER TEST

PROGRAM PURPOSE

To check that the STARLAN-DUMB line controller functions correctly.

HARDWARE REQUIRED

Starlan-dumb line controller board G0431.

INTRODUCTORY NOTES

To perform a full functional check of the Starlan-dumb controller, it must be connected to the Hub via a drop cable. If it is not, the last test (transmission and reception with loopback on the Hub) will not be performed.

LOADING PROCEDURES

Refer to section 1.3.2.

8.12.1 TEST DESCRIPTION

1) BUS TEST

The controller internal Data Bus and the Address Bus are tested by addressing, writing and reading the registers of the various controller components with specific patterns.

2) DUAL PORT MEMORY TEST

The 32 KB of dual port memory are tested. Three types of tests are run: shortcircuit test, read/write test, Abraham test.

3) PROM TEST

The node name PROM is read to verify that the PROM has been programmed correctly, and the node name is displayed.

4) INTERRUPT TEST

The interrupt handling logic is checked by verifying that interrupts are generated and that the commands connected to them are functioning correctly. The logic is tested twice; first for chain 1A and then for chain 2B.

5) LCC TEST

The LCC is tested by checking that all commands and features handled by this component function correctly.

6) LCC ALL MULTICAST ADDRESS

All the multicast address tables (64 addresses) are filled and transmission and reception is tested with all 64 addresses.

7) HUB LOOPBACK TEST

The transmission and reception test with loopback is performed on the Hub.

NOTE

This last test is only run if the Starlan-dumb controller is connected to the Hub.

8.12.2 ERROR MESSAGES

A list of error messages is shown below. If there is a blocking error try changing the controller board.

- **NO REDYA SIGNAL DURING BOARD RESET** = After an OUT has been performed to reset the Starlan-dumb controller, the non-maskable interrupt is not generated as the REDYA signal is not present on the Olibus.
- **NODE NAME ERROR** = The node name has not been duplicated in the PROM.
- **PROM ERROR** = All or part of the PROM cannot be read.
- **SPECIAL INTERRUPT NON OCCURRED** = The special controller interrupt (fixed vector "3E") has not been generated.
- **DISABLE INTERRUPT COMMAND FAULTED** = Although the controller received the interrupt disable command, it continues to generate interrupts.
- **SPECIAL INTERRUPT VECTOR INCORRECT** = The special vector port read provides a value other than "3E".
- **SET/RESET BIT IP NOT OCCURRED** the Interrupt Pending bit has not been set/cleared.
- **RESET INTERRUPT LOGIC STROBE FAULTED** = Although an interrupt has been generated and not serviced, the interrupt logic reset command eliminates the pending request.
- **BUS ERROR** = Inconsistencies were found when writing to and reading from the normal interrupt vector port.
- **MEMORY TOO SHORT FOR CONFIG. PARAMETER** = During Dual Port Memory configuration, a buffer number which is too high with respect to the memory available (16/32K) is requested.
- **ERROR IN ACCESS DUAL PORT MEMORY** = The I/O initialization routine cannot access the Dual Port Memory.
- **ERROR IN INIT RETURN PARAMETER** = The I/O initialization routine returns a wrong parameter.
- **LCC INTERRUPT NOT OCCURRED** = The LCC does not generate the interrupt.

- **RESET LCC NOT ACQUIRED** = The LCC does not accept the software reset.

- **LCC COMMAND NOT ACCEPTED** = The LCC does not accept the command sent to it.

- **UNDEFINED INTERRUPT** = The LCC generates an interrupt without just cause.

- **COMMAND UNIT STILL READY** = A command which should leave the command unit not ready leaves it ready.

- **COMMAND NOT EXECUTED** = The command issued to the LCC has not been executed.

- **RX UNIT NOT READY INT. NOT EXPECTED** = An unexpected "Rx unit not ready" interrupt has been received.

- **FRAME RX INT. NOT EXPECTED** = An unexpected "frame received" interrupt has been received.

- **DIAGNOSE RESULT FAILED** = The result of the DIAGNOSE command on the LCC is negative.

- **CABLE ABSENCE NOT NOTICED** = The operator has declared that the transceiver is not connected but the TDR test does not agree.

- **CARRIER SENSE LOST DURING TX** = During transmission of a frame, the LCC signals the loss of the carrier.

- **CTS LOST DURING TX** = During transmission of a frame, the LCC signals the loss of the CTS.

- **TX/RX DMA UNDERRUN** = During transmission/reception of a frame, the LCC signals a DMA "underrun".

- **COLLISION OVERRUN** = During transmission of a frame, the LCC signals that the maximum number of 15 collisions has been exceeded.

- **HUB BROKEN** = During a transmission and reception test, the LCC signals an error on the Hub.

- **RX INT. NOT OCCURRED** = The expected receive interrupt is not generated.

- **FRAME DESTINATION ADDRESS INCORRECT** = An error has occurred in the destination address of a received frame.

- **FRAME DATA CHARACTERS INCORRECT** = Errors have occurred in the data field of a received frame.

- **TX MESSAGE TOO SHORT/LONG** = The frame to transmit is shorter/longer than the minimum length allowed by the Ethernet 802.3 standard.

- **RX FRAME TOO SHORT** = The received frame is shorter than the minimum length allowed by the Ethernet 802.3 standard.

- **STORING FRAME NOT COMPLETED** = The LCC indicates that it has not finished storing the incoming frame.

- **ERROR IN BUFFER CHAINING** = The LCC indicates that a problem has occurred during the linking of the buffers which are to contain the received frame.

- **FRAME ALIGNMENT ERROR** = An alignment error has occurred during reception of a frame.

- **NO MEMORY RESOURCES DURING RX FRAME** = During reception of a frame, there was not enough memory space to store the frame.

- **FRAME CRC ERROR** = A CRC error has occurred in a received frame.

- **RNR INTERRUPT NOT OCCURRED** = The expected "Receive Unit Not Ready" interrupt was not generated.

- **CNR/CX INTERRUPT NOT EXPECTED** = An unexpected "Command Unit Not Ready"/"Command Execution" interrupt was generated.

- **FRAME SOURCE ADDRESS INCORRECT** = The frame source address is incorrect.

- **CRCERRS/ALNERRS COUNTER NOT CORRECTED** = The value of the CRC/alignment error counter is not 0.

- **RSCERRS/ALNERRS COUNTER NOT CORRECTED** = The value of the "memory failure"/"overrun" error counter is not 0.

- **HASH OR ADDRESS REGISTER NOT CORRECTED** = The "hash table" read, following a dump command, is not correct.

- **CABLE OR HUB PROBLEM IDENTIFIED** = The TDR test has detected faults in the drop cable or Hub.

- **ERROR DURING COMMAND EXECUTION** = An unidentified error has occurred during the execution of a command.

- **COLLISION NOT VERIFIED** = The expected collisions did not occur during the COLLISION TEST.

9. INTELLIGENT LINE TEST PROGRAMS

9.1 ER2005: LION 200 ERROR RATE EVALUATION PROGRAM

PROGRAM PURPOSE

To evaluate the error rate in exchanges of messages between line controllers, one of which is a master and the remainder slaves (maximum 31) connected by a LION network.

HARDWARE REQUIRED

2 to 32 M30/M40/60 systems, each comprising CPU board, RAM board and LION 200 controller, interconnected via a LION network.

PRELIMINARY WARNING

For the tests to be significant, the program must be loaded with the slave workstation(s) connected.

OPERATING PROCEDURE

Refer to section 1.3.2.

9.1.1 TEST DESCRIPTION

TEST WITHOUT MESSAGE RETURN

A series of messages is transmitted to each slave controller included in the test during the pre-programming stage. On receipt of the test message the slave examines the message and flags any errors detected as an error message on the VDU. The test is repeated as set in the pre-program MESS NUMBER option. This option if set to 0 forces the program into a test loop which is interrupted when SKIP is hit.

TEST WITH ACKNOWLEDMENT RETURN.

A series of messages is transmitted to each slave included in the test during the pre-programming stage. Each slave examines the test message for errors and if there are none the slave transmits an acknowledgement to the master controller. The test is repeated as set in the pre-program MESS NUMBER option. This option if set to 0 forces the program into a test loop which is interrupted when SKIP is hit.

TEST WITH MESSAGE RETURN.

A series of messages is transmitted to each slave included in the test during the pre-programming stage. Each slave examines the test message for errors and if there are none transmits a similar message to the master controller. The master controller then tests messages received and flags any errors detected. The test is repeated as set in the pre-program MESS NUMBER option. This option if set to 0 forces the program into a test loop which is interrupted when SKIP is hit.

9.1.2 STATUS/ERROR MESSAGES

In case of errors verify connection between master and slave, check/change controllers.

GENERAL MESSAGES

- LION 200 NOT READY

  Indicates that the controller is not ready to accept a command or that there is an error in the first stages of the pre-program.

- LION 200 BUSY

  Indicates that the controller, after receiving the execution command, is unable to continue as the system is not set to execute the program.

- UNKNOWN INTERRUPT ERROR

  Indicates that the controller, when set in reception, has not received an end of transmission interrupt or, when set in transmission, has not received an end of reception interrupt.

- Z-SCC DOES NOT TRANSMIT

  Indicates that after a transmission command the controller has not replied with an end of transmission interrupt.

- TX MESS.NR. xxxx TO SLAVE yy

  Indicates that the system is set to transmit message number xxxx to slave yy. If the transmission is not satisfactory, an appropriate error message is displayed. This message can be suppressed by setting the pre-program MESS RUNNING DISPLAY option to 0 to optimise the test transmission time.

- RX MESS.NR. xxxx FROM MASTER yy

  Indicates that message number xxxx from master yy has been completely received. If the operation is not satisfactory an appropriate error message is displayed. This message can be suppressed by setting the pre-program MESS RUNNING DISPLAY option to 0 to optimise the test transmission time.

ERROR MESSAGES DURING RUN TIME

Reception of incomplete messages are not signalled out with an error message or indicated in the summary status table. One of the following error messages is displayed if a completed message is received containing an an error:

- MESS. NR. (xxxx) /KO
- ACK. NR. (xxxx) TX FROM SLAVE (yy) /KO
- MESS.NR. (xxxx) TX FROM SLAVE (yy) /KO

The status message can be followed by one of the following error messages:

- CRC HEAD ERROR
- PARITY ERROR
- CRC/FRAMING ERROR
- RX OVERRUN ERROR
- OVERFLOW RX ERROR
- UNKNOWN INTERRUPT ERROR

These indicate respectively: CRC head of message error, parity transmission/ reception error, CRC or framing error, overrun error, overflow in reception buffer and error due to an unprogrammed vectored interrupt.

SUMMARY OF MESSAGES OBTAINABLE FROM EACH SLAVE CONTROLLER

When the reception/transmission of a slave controller is interrupted by pressing the SKIP key, or at the end of the test program, the system produces the following status table:

```
*****************************************
*                                       *
*   -RX MESSAGES                (1)     *
*   -RX ERROR MESSAGES          (2)     *
*   -TX MESSAGES                (3)     *
*   -CRC HEAD MESS. ERROR       (4)     *
*   -RX OVERRUN     ERROR       (5)     *
*   -PARITY         ERROR       (6)     *
*   -CRC/FRAMING    ERROR       (7)     *
*   -OVERFLOW RX    ERROR       (8)     *
*   -UNKNOWN INT.   ERROR       (9)     *
*                                       *
*****************************************
```

WHERE: (1) = the number of correctly received messages,
(2) = the number of incorrectly received messages,

(3) = the number of re-transmitted messages,
(4) = the number of CRC error messages received in the first four bytes,
(5) = the number of overrun errors,
(6) = the number of parity errors,
(7) = the number of frame or crc errors,
(8) = the number of overflow errors in reception buffer,
(9) = the number of unaccountable interrupts.

SUMMARY OF MESSAGES OBTAINABLE FROM THE MASTER CONTROLLER

TYPE 1

At the end of the test the following status table is produced for each slave controller:

```
**************************************
*                                    *
*   SLAVE NUMBER              xx     *
*   -TX MESSAGES              yy     *
*                                    *
**************************************

    HIT "ENTER" TO CONTINUE
    OR "SKIP" FOR NEXT SLAVE
```

WHERE: yy = number of messages transmitted to slave xx.

Hit ENTER to exit from program or hit SKIP to continue test on next slave controller.

TYPE 2

At the end of the test the following status table is produced for each slave controller:

```
**************************************
*                                    *
*   SLAVE NUMBER              xx     *
*   -TX MESSAGES              yy     *
*   -RX ACKNOWLEDGE           zz     *
*   -RX ERROR ACK             ww     *
*                                    *
**************************************

    HIT ENTER TO CONTINUE
    OR SKIP FOR NEXT SLAVE
```

WHERE: yy = the number of messages transmitted to slave xx,
zz = the number of acknowledgements received,
ww = the number of acknowledgements not received.

TYPE 3

At the end of the test the following status table is produced for each slave controller:

```
**************************************
*                                    *
*  SLAVE NUMBER                (1)   *
*  -TX MESSAGES                (2)   *
*  -RX MESSAGES                (3)   *
*  -RX ERROR MESSAGES          (4)   *
*  -CRC HEAD MESS. ERROR       (5)   *
*  -RX OVERRUN     ERROR       (6)   *
*  -PARITY         ERROR       (7)   *
*  -CRC/FRAMING    ERROR       (8)   *
*  -OVERFLOW RX    ERROR       (9)   *
*  -UNKNOWN INT.   ERROR      (10)   *
*                                    *
**************************************

   HIT" ENTER" TO CONTINUE
   OR "SKIP" FOR NEXT SLAVE
```

WHERE: (2) = the number of messages transmitted to slave (1),
(3) = the number of messages received correctly,
(4) = the number of messages received incorrectly,
(5) = the number of messages received with an CRC error in the first four bytes,
(6) = the number of overrun errors,
(7) = the number of parity errors,
(8) = the number of frame or CRC errors,
(9) = the number of overflow errors in reception buffers,
(10) = the number of unaccountable interrupts.

Hit ENTER to exit from program or hit SKIP to continue test on next slave controller.

9.2 ERS205: LINE CONTROLLER GO340 TEST PROGRAM

PROGRAM PURPOSE

This program is designed to test two or more inter-connected line controllers.

Error rates for the line and for connections between two controllers can also be evaluated.

The test is carried out on a series of cluster-connected, twin-line LION200 controllers (max. 32), handled in polling-selecting mode.

HARDWARE REQUIRED

CPU board, system memory, video/keyboard controller, floppy-disk controller, GO340 line controllers or via MUX (GO 322).

PRESETTINGS

The controllers should be inserted in different machines and connected on line.

The test program should first be loaded on the Slave machine and then on the Master.

NOTE

In order to visualise data exchanges it is necessary to access MONITOR HELP and set parameter 14 to 1 for EXTENDED MESSAGES.

OPERATING PROCEDURE

Refer to section 1.3.2.

9.2.1 TEST DESCRIPTION

There are 3 types of test; only one type can be selected at a time.

TEST 1: TEST WITHOUT MESSAGE RETURN

In this type of test, the Master sends a series of messages to each of the slaves declared in the pre-program.

After receiving the message, the slave checks it and signals any errors on the video.

The send cycle is repeated the number of times specified by the operator in the pre-program.

TEST 2: TEST WITH ACKNOWLEDGE RETURN

In this type of test, the Master sends a series of messages to each of the slaves declared in the pre-program.

After receiving a message, the slave checks it and sends back an acknowledgement.

The send cycle is repeated the number of times specified by the operator in the pre-program.

TEST 3: TEST WITH MESSAGE RETURN

In this type of test, the Master sends a series of messages to each of the slaves declared in the pre-program.

After receiving the message, the slave checks it and sends a similar message back to the Master, who, in turn, checks the message received.

The purpose of this test is to check out the line in master-slave and slave-master exchanges.

The send cycle is repeated the number of times specified by the operator in the pre-program.

9.2.2 ERROR MESSAGES

In case of errors verify connection between master and slave, check/change controllers.

The error messages output are listed below:

LION 200 NOT READY

The line controller has not decared itself ready to accept a command or has signalled errors in the first autodiagnostic phase.

LION 200 BUSY

After receiving a code process command loaded earlier in the dual port memory, the line controller has not declared itself busy signifying that the system is not set for program execution.

UNKNOWN INTERRUPT ERROR

With the controller set up for reception, an end-of-transmission interrupt has occurred (or vice-versa).

Z-SCC DOES NOT TRANSMIT

On a transmit command, the controller has not responded with the end-of-transmission interrupt.

MESS.NR. xxxx TO SLAVE yy

The system is set for transmission of message no. (xxxx) to slave (yy).

If the operation is not succesful, an error message is produced.

This message appears on the diagnostic console and may be omitted by way of a pre-program option.

If the option is omitted, the console line can be used throughout.

RX MESS.NR. xxxx FROM MASTER yy

message no. (xxxx) has been received from Master (yy).

Remarks made for the previous message also apply here.

******** RUN TIME ERROR MESSAGES ********

Incomplete messages are not accompanied by error messages as it is impossible to distinguish aborted messages from line noise.

Incomplete messages are not counted in the overall summary.

A complete but incorrect message is accompanied by one of the following messages:

MESS. NR (xxxx) /KO

ACK. NR. (xxxx) TX FROM SLAVE (yy) /KO

MESS. NR. (xxxx) TX FROM SLAVE (yy) /KO

The type of error will also be given, if the option is selected in the pre-program phase.

Typical errors are:

CRC HEAD ERROR

PARITY ERROR

CRC/FRAMING ERROR

RX OVERRUN ERROR

OVERFLOW RX ERROR

End of reception interrupts may in some cases be lost during a diagnostic monitor display, even though the message is short.

It is, therefore, advisable to omit the error explanation option as the errors are in any case included in the final summary.

9.3 L2V248: LCU V24 + LION 200 CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To check line controller operation, by running a number of tests on the Olibus interface, the CPU, the ROM, RAM and management of the two serial channels.

HARDWARE REQUIRED

CPU board, RAM board, V24 + LION 200 controller (G0256)

PRELIMINARY WARNING

Before running the test observe the following:

a) Disconnect any external devices serially connected to the controller.

b) If test is run with an external loop, connect plugs to the controllers with links as shown below.

c) Ensure correct memory size is available for the tests (default 8K words).

d) Ensure correct default values are set in the preprogram.

EXTERNAL LOOP CONNECTION

If the test is run with an external loop, two plugs are needed to produce the hardware loop on the controller boards. Connect as shown below:

```
BOARD UNDER TEST                          AUXILIARY BOARD

PIN 1 to PIN 2 to PIN 3
PIN 4 to PIN  7,
PIN 8 to PIN 11 to PIN 13
PIN 9 to PIN 17
PIN 12 to PIN 15
PIN 25 ------------ to --------------> PIN 25
PIN 26 ------------ to --------------> PIN 26
PIN 1 to PIN 2 to PIN 3
PIN 4 to PIN  7,
PIN 8 to PIN 11 to PIN 13
PIN 9 to PIN 17
PIN 12 to PIN 15
```

OPERATING PROCEDURE

Refer to section 1.3.2.

9.3.1 TEST DESCRIPTION

MEMORY INITIALIZATION TEST

This test examines the basic operation of the controller, by checking first RAM initialization and then the controller busy status. When no errors are found, the next test is run.

MEMORY (HOST) TEST

Checks operation of the dual-port memory as host. The test is in three separate parts:

- a number of consecutive reads and writes (at bus cycle level) are performed in order to discover the critical points of access times.
- a check for short circuits on the memory word.
- the "comparison" test.

When no errors are found, the next test is run.

Z8002 TEST

A check on the Z8002 microprocessor operation. Checks are run on the instructions involving internal operations. When no errors are found, the next test is run.

MEMORY TEST (SLAVE)

A check on the internal operation of the dual-port memory and bus drivers. The operations carried out are the same as in the equivalent host memory test. When no errors are found, the next test is run.

ROM TEST

The ROM controller is tested. The CRC is taken and compared with the value stored in the ROM. When no errors are found, the next test is run.

INTERRUPT TEST

The interrupt vector load operations are checked out. The test also ensures that the controller being tested is the only source of interrupt. When no errors are found, the next test is run.

Z-CIO (TIMERS)

The timers are checked in their three possible modes of operation: pulse output, one shot output and square wave output. Where possible, the timers are cascade-connected. When no errors are found, the next test is run.

Z-CIO (PARALLEL I/O)

This checks that the Z-CIO parallel ports are functioning correctly. A number of write operations are performed, followed by read operations to ensure that the individual line handling signals are correct. When no errors are found, the next test is run.

LINE DRIVERS TEST

A check on the line drivers (CHANNEL B only) and their circuits. The baud rate generator and all possible line signal paths are tested. When no errors are found, the next test is run.

Z-SCC TEST (CHANNEL A/B)

The LSI Z-SCC component and the logic of the related lines are tested by checking that the reception/transmission channels function correctly. When there are no errors, the next test is run.

INTERNAL INTERRUPT TEST

The controller's internal daisy chain is tested by checking that all devices in the daisy chain are enabled correctly using the interrupt logic. When there are no errors, the next test is run.

TX/RX LOCAL LOOP TEST

A reception/transmission test is run simultaneously on channel B at a higher speed than normal.

LINE LEDS TEST

A test is made on the DCD, DSR and RTS LEDs whereby the LEDs are switched on and off for approximately two seconds and messages displayed to indicate LED status (see next section for LINE LED STATUS MESSAGES).

ACTIVE LOOP TEST

Data is exchanged and tested on channel A between two line controllers (the controllers can be in the same machine or in two different machines).

9.3.2 ERROR MESSAGES

In case of errors replace the controller board unless otherwise indicated.

The program provides the following error messages which can be displayed as a single message or a number of messages as a result of specific tests.

SYSTEM DISABLING MESSAGES

- *** PRIVILEGE INSTRUCTION TRAP *** = execution in user mode of a privilege instruction.

- *** SEGMENT TRAP = access of memory area not managed by the MMU

- *** ILLEGAL MEMORY TRANSACTION *** = accesss of memory area not present.

- LCU ..... = parameters provided by Pascal sub-system modules out of tolerance.

TIME OUT MESSAGES

- TIME OUT: LION200+V24 NOT READY = controller not ready.
  SELF DIAGNOSTIC RESULT IS (XXXX)

- TIME-OUT: PROGRAM NOT RUNNING = test not in progress.

- TIME-OUT: BAD END PROGRAM = current test time-out elapsed or incorrect cycle(s) on controller bus.

- DUAL PORT-MEMORY NOT READY = "redya" signal not present in a dual-port memory access.

DIAGNOSTIC MESSAGES

- LION200 (UNDER TEST) BUSY/NOT READY = controller under test busy/not ready.

- LION200 (ACTIVE LOOP) BUSY/NOT READY = controller selected in active loop not busy/not ready.

- END TRANSMISSION/RECEPTION OF BOARD UNDER TEST/ACTIVE LOOP = end of transmission/reception interrupt signalled on board with active loop

- ERROR ON MEMORY INITIALISATION = error on initialization of the RAM by the controller.
  VERIFY THE ADDRESS LINE NUMBER (XX) ....(YY)

- ERROR ON ODD/EVEN/ALL BLOCK(S) = error on the odd/even/all ROM address(es)

- TEST NOT FINISHED = possible faults on the RAM slave chips in addition to those already signalled.

- ERROR ON CHIP 1/2/3/4 (LOW AND ODD/EVEN or HIGH AND ODD/EVEN) = error on chip indicated for LOW/HIGH RAM addresses and ODD/EVEN bytes

- CPU TEST ERROR = incorrect instruction execution of the CPU Z8002 .

- NOT INTERRUPT = controller not interrupting the system CPU.

- BAD INTERRUPT VECTOR = interrupt vector incorrect.

- FAILURE ON PARALLEL I/O = fault on the parallel ports of the chips specified by the following error message.

- Z-CIO 1/2 = Z-CIO 8036 dedicated to channel A/B.

- Z-CIO 1 & 2 = both Z-CIO 8036s.

- Z-CIO 1/2 TIMER N.X = fault in timer no. X, dedicated to channel A/B.

- BAD CLOCK OR ERROR ON COUNTING = error on counter or controller clock.

- ERROR ON RECEIVED BLOCK = error on data received.

- RX/TX NOT READY = receiver/transmitter not ready after time-out has elapsed.

- INTERNAL LSI LOOP = with an internal Z-SCC loop.

- EXTERNAL/ON BOARD LOOP = indicates associated with loop plug/internal loop.

- *** CHANNEL "A/B" *** = indicates messages which follow refer to channel A/B.

- BAUD RATE GENERATOR = baud rate fault in specified channel.

- UNDEFINABLE FAILURE = interrupt received, other than the one expected during the interrupt test.

- FAILURE ON INTERNAL INTERRUPT/DAISY CHAIN

- Z-SCC = the faults described above can be attributed to the Z-SCC 8030.

- INTERFACE SIGNAL FAILURE = malfunctions in certain signal pairs, listed below:

  103/107 = data tx/DSR
  111/125 = rate selector/ring indicator
  141/142 = local loop back/test indicator
  105/106 = RTS/CTS
  108/109 = DTR/DCD

- FAILURE ON DIAGNOSTIC LOOP = errors due to tests on the above signals with loop connected on the controller.

- ERROR NUMBER (X) = malfunction on one or more logic chains, obtained by using the internal "on board" loop plug (x is a number between 1 to 7).

- TRANSMITTER/RECEIVED TIME OUT = time-out in transmission/reception.

- RX PARITY/OVERUN/FRAMING ERROR = parity error in data received/characters lost in reception/SDLC protocol error.

- UNKNOWN INTERRUPT = an interrupt served on an unprogrammed vector or an unexpected interrupt.

- **WARNING MESSAGES**

- *** WARNING EXTERNAL LOOP *** = any error signals which can be attributed to the absence of the loop plug will be omitted.

- ** WARNING TEST SKIPPED ** = test requested by the operator not run.

- **LINE LED STATUS MESSAGES**

```
ALL LEDS OFF      =  DCD OFF;  DSR OFF;  RTS OFF
DCD      ON       =  DCD ON ;  DSR OFF;  RTS OFF
DSR      ON       =  DCD OFF;  DSR ON ;  RTS OFF
RTS      ON       =  DCD OFF;  DSR OFF;  RTS ON
ALL LED  ON       =  DCD ON ;  DSR ON ;  RTS ON
DCD      OFF      =  DCD OFF;  DSR OFF;  RTS OFF
DSR      OFF      =  DCD ON ;  DSR OFF;  RTS ON
RTS      OFF      =  DCD ON ;  DSR ON ;  RTS OFF
COFFN    OFF      =  DCD OFF;  DSR OFF;  RTS OFF (sig. at logic level 1)
COONN    OFF      =  DCD OFF;  DSR OFF;  RTS OFF (sig. at logic level 1)
COFFN    ON       =  DCD ON ;  DSR ON ;  RTS ON  (sig. at logic level 0)
COONN    ON       =  DCD ON ;  DSR ON ;  RTS ON  (sig. at logic level 0)
```

9.4 V24L27: LINE CONTROLLER BOARD G0340 TEST PROGRAM

PROGRAM PURPOSE

This program is designed to check operation of the G0340 line controller by running tests on the OLIBUS interface, the CPU, ROM and RAM storage and by testing the hardware of the two serial channels.

Testing can take three forms:

a) with G0340 in stand alone

b) with G0340 line controller test connected through loop plugs to another G0340 line controller in the same unit

c) with G0340 line controller test connected on line to another G0340 line controller in a second unit

HARDWARE REQUIRED

CPU board, RAM board, video/keyboard controller, one or two G0340 line controllers.

PRESETTINGS

For this program, an external loop plug must be used on the serial line.

Connect the 2 X 15-way, 100 mm connectors as shown below:

```
Plug no 1                                   Plug no 2
Pin connections:                            Pin connections:
1-A   1-B   2-D   3-C
4-F   4-H   6-J   K-E
                    P----------------------->P
                   13----------------------->13
```

The following operations must also be carried out:

a) Remove all external serial connections to controller

b) Fit loop plug, if required

c) Check the controller memory space

d) Check that the programmed memory is correct

OPERATING PROCEDURE

Refer to section 1.3.2. for general operating procedure, and in addition, observe the following:

1) For stand alone line controller G0340

- Fit Loop plug no. 1 and leave plug no. 2 free.

NOTE:

If the plug is not fitted, the following tests are omitted:

- LINE DRIVER CH.B
- TX/RX LOCAL LOOP
- LINE LEDS TEST
- ACTIVE LOOP CH.A

2) Line controller G0340 test using a sample line controller G0340 in the same machine.

- Fit plug no. 1 on the line controller to be tested and plug no. 2 on the auxiliary (sample) line controller.

NOTE

All tests are carried out if response given to LINE LEDS TEST? is 1; if the response is 0, only the test on the LEDs is omitted.

3) Line controller G0340 test using an auxiliary line controller G0340 in another machine.

The two controllers must be connected on a line.

NOTE

The following tests are not carried out:

- LINE DRIVER CH. B
- Tx/Rx LOCAL LOOP
- LINE LEDS.

9.4.1 TEST DESCRIPTION

The test performed is as described in the L2V248 program, section 9.3.1.

9.4.2 ERROR MESSAGES

The error and warning messages are the same as described in section 9.3.2.

9.5 W24D08: LCU V24 + V24 CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

To check line controller operation, by running a number of tests on the Olibus interface, the CPU, the ROM, RAM and management of the two serial channels.

HARDWARE REQUIRED

V24 + V24 controller (G0236).

PRELIMINARY WARNING

a) Disconnect any external devices serially connected to the controller.

b) Ensure correct memory size is available for the tests (default 8K words).

c) Ensure correct default values are set in the preprogram.

EXTERNAL LOOP CONNECTION

If the external loop test is required, fit plug on controller's 15 X 2 way 100 mm connector wired as shown:

PIN 1 to PIN A to PIN B
PIN 2 to PIN D
PIN 3 to PIN C
PIN 4 to PIN F to PIN H
PIN 6 to PIN J
PIN E to PIN K
PIN 7 to PIN 11
PIN 8 to PIN L
PIN 9 to PIN 10 to PIN N
PIN 12 to PIN R
PIN 13 to PIN P
PIN 14 to PIN 15 to PIN S

LOADING PROCEDURE

Refer to section 1.3.2.

9.5.1 TEST DESCRIPTION

The test performed is as described in the L2V248 program, section 9.3.1 except for the ACTIVE LOOP TEST which is omitted. Also the LINE DRIVER TEST and the TX/RX LOCAL LOOP TEST in this program apply to both channels A and B.

9.5.2 ERROR MESSAGES

Refer to section 9.3.2. (except for the messages which refer to the L1ON 200 controller).

9.6 W24S07: LPU V24 + V24 (SHARED SEGMENT) TEST PROGRAM

PROGRAM PURPOSE

The program is designed to check operation of the controller.

HARDWARE REQUIRED

V24 + V24 (shared segment) LCU board G0331.

WARNING

Before starting the test, set up the controller board as described:

1. Remove any external serial connections
2. Insert the loop plug, if required
3. Check the controller storage available
4. Check that the programmed memory size is correct

EXTERNAL LOOP CONNECTION

Fit plug, with pins connected as indicated below:

1-A	1-B	2-D	3-C
4-F	6-J	7-11	8-L
9-10	10-N	12-R	13-P
14-15	15-S	E-K	

OPERATING PROCEDURE

Refer to section 1.3.2.

9.6.1 TEST DESCRIPTION

The test performed is as described in the L2V248 program, section 9.3.1 except for the ACTIVE LOOP TEST which is omitted. Also the LINE DRIVER TEST and the TX/RX LOCAL LOOP TEST in this program apply to both channels A and B.

9.6.2 ERROR MESSAGES

The error and warning messages are the same as described in section 9.3.2. except for the messages which specifically refer to the L10N 200 controller.

9.7 L9V244: LINE CONTROLLER BOARD G0340/A TEST PROGRAM

PROGRAM PURPOSE

This program is designed to check operation of the G0340/A line controller by running tests on the OLIBUS interface, the CPU, ROM and RAM and testing the hardware of the two channels.

The following types of test are possible:

a) Stand alone G0340/A testing

b) G0340/A testing via another G0340/A in the same machine and connected to the first by loop plugs.

c) G0340/A testing via another G0340/A in another machine and connected to the first on line.

HARDWARE REQUIRED

CPU board, RAM board, video/keyboard controller, one or two G0340/A controllers.

GENERAL

This program is the same as the V24L27 program, section 9.4, except that it is used to check the G0340/A controller. Reference should therefore be made to the V24L27 program for PRESETTINGS and LOADING PROCEDURE substituting G0340 for G0340/A when reading the text.

9.7.1 TEST DESCRIPTION

Refer to the L2V248 program, section 9.3.1.

9.7.2 ERROR MESSAGES

Refer to section 9.3.2.(except messages which specifically refer to the LION 200 controller)

9.8 MOW240: MOIN52 TEST PROGRAM WITH V24 + V24 LINE CONTROLLER

PROGRAM PURPOSE

The program is intended to check out operation of the modem MOIN 5.2 when used in connection with the intelligent line controller G0331.

HARDWARE REQUIRED

CPU board, RAM board, video/keyboard controller, floppy disk unit, V24 + V24 intelligent line controller (G0331) and modem MOIN 5.2.

PRE-SETTINGS

The line controller and modem are to be connected by a connection cable.

The two Dual line, 15-way, 100 mm connectors must be connected as indicated in the service manual:

OPERATING PROCEDURE

Refer to section 1.3.2.

9.8.1 TEST DESCRIPTION

See section 8.5.1 of the MOINV2 test program.

9.8.2 ERROR MESSAGES

In case of errors verify connection between master and slave, check/change controllers.

There are two types of error message:

- for blocking errors
- for non-blocking errors

The following messages refer to blocking errors:

- TIME OUT: V24 + V24 NOT READY
- TIME OUT: PROGRAM NOT RUNNING
- TIME OUT: BAD END PROGRAM
- DUAL PORT MEMORY NOT READY

The preceding messages may, in some cases, be accompanied by the message:

- SELF DIAGNOSTIC RESULT IS XXXX

where XXXX is the line controller autodiagnostic result.

All the above message refer to the V24 + V24 line controller; they do not refer to the board being tested.

Messages referring to non-blocking errors are:

- RX NOT READY
- TX NOT READY

  when the transmitter or receiver are not in sync.

- CTS ON NOT OCCURRED
- CTS OFF NOT OCCURRED
- DCU ON OCCURRED

  when the DCU and CTS signal transitions do not occur

- ERROR IN MODEM TO CONNECT TO LINE

  modem cannot be connected to line

- MODEM NOT CONNECTED TO LINE

  modem should be connected, yet declares it is not

- MODEM INTERNAL LOOP NOT ACTIVE

  when the modem cannot be set for diagnostic operations

- MODEM INTERNAL LOOP ALWAYS ACTIVE

  when modem cannot be taken out of diagnostic mode.

9.9 ETHER2: EHERNET ERROR RATE TEST PROGRAM

PROGRAM PURPOSE

The program is intended as a functional check of the ETHERNET line and to reveal the error rate.

HARDWARE REQUIRED

G0212A controller board(s), Ethernet line.

HARDWARE SETTINGS

The controller is connected to the transceiver by a drop cable; the transceiver is then connected to the Ethernet.

N.B.

The controllers under test are connected to the network via telephone lines; each controller in an NLS3000 or NLS8000 system is defined as a station. A number of stations (or NODES) can be connected depending on the system memory space available on the MASTER or CONTROL station for storing statistical data. In this program, the number of stations has been limited to 128.

CAUTION
It is necessary to run the program on the slave stations and then on the master station.

OPERATING PROCEDURE

Refer to section 1.3.2.

9.9.1 TEST DESCRIPTION

The test description is the same as that given for the STARLO program, section 8.11.1, with the following exceptions:

- STARLINE should read ETHERNET
- co-axil cable should read telephone cable
- HUB should read TRANSCEIVER or ESI (Ethernet Serial Interface).

9.9.2 SERVIVCE, ERROR AND SUMMARY MESSAGES

Refer to section 8.11.2.

9.10 OMNIN4: DEDICATED OMNINET LINE CONTROLLER TEST PROGRAM

PROGRAM PURPOSE

The program is designed to check out the OMNINET line controller.

The checks carried out are:

a) OMNINET G0308 board check.

b) A check of two controllers connected via an OMNINET network (a second unit is required).

c) A check of two controllers in the same unit and connected via loop plugs.

OPERATING PROCEDURE

Refer to section 1.3.2.

HARDWARE REQUIRED

OMNINET board G0308, drop cable, OMNINET network.

9.10.1 TEST DESCRIPTION

The test consists of transmitting and receiving specific data packets of various lengths and analysing the results.

9.10.2 MESSAGES OUTPUT

If there is a blocking error verify connection between controllers, verify/change controller boards.

Messages output and their significance are listed below:

1. ENTER "SKIP" TO EXIT
2. WARNING BOARD TESET ERROR
3. AT ADD. XXXX READ YY EXPECTED ZZ
4. AT ADD. XXXX DUAL PORT MEMORY NOT READY
5. *** PRIVILEGED INSTRUCTION TRAP ***
   LOCATION COUNTER : XXXX
6. *** SEGMENT TRAP ***
   LOCATION COUNTER : XXXX
7. *** NON MASKABLE INTERRUPT ***
   LOCATION COUNTER : XXXX
8. STATUS/CONTROL REGISTER NOT READY
   LOCATION COUNTER : XXXX
9. XXXX IS A BAD VECTOR
10. NO INTERRUPT
    I HAVE TRIED VECTOR XXXX

11. TESTED NODE NAME XX
12. WHO AM I COMMAND TIMEOUT ERROR
13. WHO AM I TEST ERROR
14. MAXIMUM NUMBER OF RETRY XX
15. NUMBER OF CLOSING FLAGS XX
16. SCALE FOR RANDOM DELAY
17. WRONG POKE OPERATION
18. PEEK COMMAND TIMEOUT ERROR
19. POKE COMMAND TIMEOUT ERROR
20. I/O TEST ERROR
21. MESSAGE NOT ACKNOWLEDGED
22. MESSAGE DATA FIELD TOO LONG
23. UNITIALIZED DESTINATION SOCKET
24. INCORRECT MESSAGE CONT. FIELD LENGHT
25. INVALID SCOCKET NAME
26. SOCKET IN USE
27. INCORRECT NODE NUMBER
28. WRONG SETUP RECEIVE (BOARD UNDER TEST)
29. WRONG SETUP RECEIVE (ACTIVE LOOP)
30. TX TIME-OUT (BOARD UNDER TEST)
31. RX TIME-OUT (BOARD UNDER TEST)
32. TX TIME-OUT (ACTIVE LOOP)
33. RX TIME-OUT (ACTIVE LOOP)
34. END OF TRANSMISSION (BOARD UNDER TEST)
35. END OF RECEPTION (BOARD UNDER TEST)
36. END OF TRANSMISSION (ACTIVE LOOP)
37. END OF RECEPTION (ACTIVE LOOP)
38. UNATTENDED INTERRUPT
39. XXXX CHARACTERS TRANSMISSION
40. RETRY NUMBER XX
41. UNRICOGNIZED ERROR
42. RAM TEST (0000 - 0FFF)
43. RAM TEST (1000 - 1FFF)

Message no. 1 is output by the program operating the auxiliary unit.

Message no. 2 indicates a board reset error.

Message no. 3 refers to the dual port memory test and indicates that data read and data written do not tally. XXXX is the address the error has been found at, YY the data read and ZZ the data written.

Message no. 4 refers to the dual port memory test and indicates that memory address XXXX cannot be accessed.

Message nos. 5, 6, 7 and 8 indicate system errors.

Message no. 9 refers to the special interrupt test and indicates that the interrupt vector found, XXXX, is not the one expected.

Message no. 10 is output when the special interrupt does not occur. XXXX is the interrupt vector expected.

Message no. 11 is output in the WHOAMI test when the test with node name XX is performed correctly.

Message no. 12 indicates that the WHOAMI command has still not been processed by the controller 1 second after issue of the command.

Message no. 13 is output to represent an error in the WHOAMI test.

Message no. 14 refers to the Peek/Poke test: XX is the default data (no. of re-attempts to send) read.

Message no. 15 refers to the Peek/Poke test: XX is the default data (no. of closing flags) read.

Message no. 16 refers to the Peek/Poke test: XX is the default data (no. of XXXXXXXXXXXXXXXX) read.

Message no. 17 refers to the Peek/Poke test and indicates a discrepancy between the data written (Poke) and data read (Peek).

Message no. 18 refers to the Peek/Poke test and indicates that the Peek command has still not been processed by the controller 1 second after issue of the command.

Message no. 19 refers to the Peek/Poke test and indicates that the Poke command has still not been processed by the controller 1 second after issue of the command.

Message no. 20 indicates an error in the I/O test.

Message no. 21 is output by the transmitting controller in the send/receive test when the message sent out is not received by the receiving controller. Message no. 22 is output by the transmitting controller in the send/receive test when the receiving controller receives a message longer than programmed length.

Message no. 23 is output by the transmitting controller in the send/receive test to indicate that the receiving controller is not initialized.

Message no. 24 is output by the transmitting controller in the send/receive test and indicates a control message error.

Message no. 25 is output in the send/receive test to indicate that the target socket has been given an incorrect name.

Message no. 26 is output in the send/receive test to indicate that a still active socket has been set for reception.

Message no. 27 is output in the send/receive test by the transmitting controller when an incorrect target node name is given in the send command issue phase.

Message no. 28 is output when an error occurs in the test board reception set-up phase.

Message no. 29 is output when an error occurs in the sample board reception set-up phase.

Messages 30 and 31 are ouput on expiry of time allowed on the test board following issue, respectively, of a send command and of a receive command.

Messages 32 and 33 are similar to messages 30 and 31, with the difference that, in this case, reference is to the sample board.

Messages 34 and 35 are output to indicate, respectively, end of transmission and end of reception on the test board.

Messages 36 and 37 are similar to messages 34 and 35, with the difference that, in this case, reference is to the sample board.

Message 38 is output when a non-scheduled interrupt occurs in the receive/ send phase.

Message 39 is output at the start of each receive/send phase. XXXX may be value 511, 1023, 1535 or 2047.

Message 40 is output by the transmitting controller when several attempts to transmit are made before the message is finally received by the receiving controller, XX being the number of attempts made.

Message 41 is output when, in a send or receive command, a signal not included in the range of possible errors is displayed.

Messages 42 and 43 are output by the unit containing the test board in the RAM test phase with simultaneous receive/send.

Message 42 refers to tests on the lower half (0-0FFF) of the dual port memory on the test board, message 43 to tests on the upper half (1000-1FFF) of the memory.

9.11 OMNSH1: SHARED OMNINET LINE CONTROLLER TEST PROGAM

PROGRAM PURPOSE

This program is designed to test operation of the OMNINET line controller. Tests may be performed in three different ways:

a) on a stand-alone OMNINET controller board

b) on two controllers on the same machine interconnected by loop plugs.

c) on two controllers interconnected on an OMNINET line (auxiliary machine required)

HARDWARE REQUIRED

One or two OMNINET line controllers connected to an OMNINET line.

The controllers may be in the same machine or in two different machines.

NOTES

1. The OMNINET controller must occupy only half the dual port memory segment.

2. The two OMNINET controllers (the one under test and the one used as sample) may be on an OMNINET line with other controllers.

3. The controllers must use different polling names.

4. The two plugs are interconnected as indicated below:

   PIN P of one plug to PIN P of the other plug
   PIN 13 of one plug to PIN 13 of the other plug

OPERATING PROCEDURE

Refer to section 1.3.2.

9.11.1 TEST DESCRIPTION

The test consists of transmitting and receiving specific data packets of various lengths and analysing the results.

9.11.2 ERROR MESSAGES

Refer to section 9.10.2 of the OMNIN4 program.

9.12 REPTRO: SHARED SEGMENT OMNINET REPEATER TEST PROGRAM

9.12.1 PROGRAM NAME: REPTRO

PROGRAM PURPOSE

To test an omninet repeater using two omninet system with shared segment controllers.

HARDWARE REQUIRED

Two omninet systems (one master the other slave), two tap boxes, a repeater box and two x 150 m length test cables. Each system with an on-board shared segment omninet controller.

CONFIGURATION

The systems are configured as follows:

- The master system with controller connected via drop cable to a tap box,
- The slave system with controller connected via drop cable to the other tap box.

The repeater must be located in the middle of the two 150 m test cables between the tap boxes.

The two ends of the trunk cable must be connected with a resistance of 110 Ohm, and 5% tolerance. The tap boxes are already set for this, and the resistors already mounted in the repeater.

N.B. The program must be run on the slave system and then on the master system. Also different polling names must be used for each controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

9.12.2 TEST DESCRIPTION

The test consists of transmitting and receiving specific data packets of various lengths and analysing the results.

9.12.3 ERROR MESSAGES

If there is a blocking error verify connection between controllers, verify/change controller boards.

- **WARNING BOARD RESET ERROR**

  This message is issued when an error occurs after a board reset.

- **AT ADD. XXXX READ YY EXPECTED ZZ**

  Issued during the dual port memory test when a different value from the one written is read. XXXX is the address at which the error is verified, YY is the value read and ZZ is the expected value.

- **AT ADD. XXXX DUAL PORT MEMORY NOT READY**

  This message is issued during the dual port memory test when the memory cell at address XXXX cannot be accessed.

- ***** PRIVILEGED INSTRUCTION TRAP *****
  LOCATION COUNTER : XXXX

- ***** SEGMENT TRAP *****
  LOCATION COUNTER : XXXX

- ***** NON MASKABLE INTERRUPT *****
  LOCATION COUNTER : XXXX
  STATUS/CONTROL REGISTER NOT READY
  LOCATION COUNTER : XXXX

  These messages are issued by the program when a system error occurs.

- **XXXX IS A BAD VECTOR**

  Issued during the special interrupt test when a different interrupt vector from the one expected is verified. XXXX is the detected vector.

- **NOT INTERRUPT**
  I HAVE TRIED WITH VECTOR XXXX

  This message is issued when the special interrupt is not verified. XXXX is the vector of the expected interrupt.

- **MESSAGE NOT ACKNOWLEDGED**

  This message is issued by the sending controller during the sending and receiving test when the message sent is not received by the target controller.

- **MESSAGE DATA FIELD TOO LONG**

  This message is issued by the sending controller during the sending and receiving test when the target controller receives a longer message than it has been programmed for.

- **INITIALIZED DESTINATION SOCKET**

  This message is issued by the sending controller during the sending and receiving test when the target controller has not been initialized.

- **INCORRECT MESSAGE CONT. FIELD LENGTH**

  This is issued by the sending controller during the sending and receiving test when an error in the control message is detected.

- **INVALID SOCKET NAME**

  Issued during the sending and receiving test when an invalid name is given for the target socket.

- **SOCKET IN USE**

  This message is issued during the sending and receiving test when an attempt is made to set a socket to receive while it is in use.

- **INCORRECT NODE NUMBER**

  Issued during the sending and receiving test when the sending controller is given an incorrect target node number while launching a transmit command.

- **WRONG SETUP RECEIVE (BOARD UNDER TEST)/(ACTIVE LOOP)**

  This message is issued by the program when an error is detected while setting up the board under test to receive.

- **TX/RX TIME-OUT (MASTER/SLAVE MACHINE)**

  These messages are issued when there is a timeout on the reference board; the first is issued after a transmit command, and the second after a receive command.

- **END OF TRANSMISSION/RECEPTION (MASTER/SLAVE MACHINE)**

  These messages are issued by the program when end of transmission and end of reception are respectively verified on the reference controller.

- **UNATTENDED INTERRUPT**

  This message is issued when an unexpected interrupt is verified during sending and receiving.

- **XXXX CHARACTERS TRANSMISSION**

  This message is issued by the program every time a sending and receiving phase is initialized; XXXX can be 511, 1023, 1535 or 2043.

- **RETRY NUMBER XX**

  Issued by the sending controller when several attempts to send are made before the message is received by the target controller; XX is the number of tries made.

- **UNRECOGNIZED ERROR**

  This message is issued when an indication which is not in the range of possible errors is included in a send or receive command.

9.13 REPTDO: DEDICATED SEGMENT OMNINET REPEATER TEST PROGRAM

PROGRAM PURPOSE

To test an omninet repeater using two omninet systems with dedicared segment controllers.

HARDWARE REQUIRED

Two omninet systems (one master the other slave), two tap boxes, a repeater box and two x 150 m length test cables. Each system with an on-board dedicated segment omninet controller.

CONFIGURATION

The systems are configured as follows:

- The master system with controller connected via drop cable to a tap box,
- The slave system with controller connected via drop cable to the other tap box.

The repeater must be located in the middle of the two 150 m test cables between the tap boxes.

The two ends of the trunk cable must be connected with a resistance of 110 Ohm, and 5% tolerance. The tap boxes are already set for this, and the resistors already mounted in the repeater.

N.B. The program must be run on the slave system and then on the master system. Also different polling names must be used for each controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

9.13.1 TEST DESCRIPTION

The test consists of transmitting and receiving specific data packets of various lengths and analysing the results.

9.13.2 ERROR MESSAGES

Refer to the REPTRO program section 9.12.2.

9.14 ETCOL4: ETHERNET CONTROLLER TEST

PROGRAM PURPOSE

To check that the ETHERNET line controller functions correctly.

HARDWARE REQUIRED

Ethernet line controller board G0212 and transceiver.

INTRODUCTORY NOTES

To perform a full functional check of the Ethernet controller, it must be connected to the transceiver via a drop cable. If it is not, the last two tests (transmission and reception with loopback on the transceiver and collision detection) will not be performed.

The transceiver must be adapted: if a 3COM transceiver is used, terminators must be installed at both ends; if an OLTECO transceiver is used, a stretch of Ethernet cable with plugs at the two ends must be connected.

LOADING PROCEDURES

Refer to section 1.3.2.

9.14.1 TEST DESCRIPTION

The test description is the same as that given for the SLANC1 program, section 8.12.1, with the following exceptions:

- STARLAN-DUMB should read ETHERNET
- HUB should read TRANSCEIVER
- test 7 is for the ESI (Ethernert Serial Interface)
- test 8 (similar to the ESI test 7) is for the TRANSCEIVER

NOTE

Test 8 and 9 are only run if the Ethernet controller is connected to the transceiver.

9.14.2 SERVIVCE, ERROR AND SUMMARY MESSAGES

Refer to section 8.12.2.

9.10 OMNSHO: OMNINET LINE CONTROLLER TEST PROGAM

PROGRAM PURPOSE

This program is designed to test operation of the OMNINET line controller. Tests may be performed in three different ways:

a) on a stand-alone OMNINET controller board

b) on two controllers on the same machine interconnected by loop plugs.

c) on two controllers interconnected on an OMNINET line (auxiliary machine required)

HARDWARE REQUIRED

CPU board, RAM board, video/keyboard controller, one or two OMNINET line controllers connected on an OMNINET line.

The controllers may be in the same machine or in two different machines.

NOTES

1. The OMNINET controller must occupy only half the dual port memory segment.

2. The two OMNINET controllers (the one under test and the one used as sample) may be on an OMNINET line with other controllers. The test does not adversely effect operation of the other controllers.

3. The TWO OMNINET controllers must have different polling names from the other controllers.

4. The two plugs are interconnected as indicated below:

   PIN P of one plug to PIN P of the other plug
   PIN 13 of one plug to PIN 13 of the other plug

OPERATING PROCEDURE

Refer to section 1.3.2.

9.10.1 TEST DESCRIPTION

The test consists of transmitting and receiving specific data packets of various lengths and analysing the results.

9.10.2 MESSAGES OUTPUT

If there is a blocking error verify connection between controllers, verify/change controller boards.

Error messages which may be output in the course of the program are listed in section 9.9.2 of the OMNIN4 program.

9.11 REPTRO: OMNINET LINE CONTROLLER REPEATER TEST PROGRAM

9.11.1 PROGRAM NAME: REPTRO

PROGRAM PURPOSE

This program is designed to provide a diagnostic aid for the omninet repeater.

HARDWARE REQUIRED

The minimum hardware essential for the execution of this program is a REPEATER and two systems, both equipped with the following modules: CPU, RAM board, video keyboard controller and a shared segment omninet line controller.

PRESETTINGS

Before executing the program, the operator must configure the two systems in the following way:

- a master system with an on-board shared segment omninet controller with a drop cable connected to the corresponding tap box;

- a slave system with an on-board shared segment omninet controller with a drop cable connected to the corresponding tap box.

The repeater to be tested must be located in the middle of two 150 m stretches of trunk cable between the tap boxes of the two systems. This configuration is the most critical for omninet installation specifications, but shorter stretches of trunk cable may also be used.

The two ends of the trunk cable must be connected with a resistance of 110 Ohm, and 5% tolerance. The tap boxes are already set for this, and the appropriate resistors are mounted in the repeater.

If the repeater to be tested is already installed, two systems on opposite sides of the repeater should be used as the master and slave.
This test does not affect any other controllers on the line, providing that the controllers of the systems used have different polling names from all the other controllers present on line.

N.B. For correct program execution, the program must be initiated on the slave system first, and then on the master system.

OPERATING PROCEDURE

Refer to section 1.3.2.

9.11.2 TEST DESCRIPTION

The test consists of transmitting and receiving specific data packets of various lengths and analysing the results.

9.11.3 ERROR MESSAGES

If there is a blocking error verify connection between controllers, verify/change controller boards.

- **WARNING BOARD RESET ERROR**

  This message is issued when an error occurs after a board reset.

- **AT ADD. XXXX READ YY EXPECTED ZZ**

  Issued during the dual port memory test when a different value from the one written is read. XXXX is the address at which the error is verified, YY is the value read and ZZ is the expected value.

- **AT ADD. XXXX DUAL PORT MEMORY NOT READY**

  This message is issued during the dual port memory test when the memory cell at address XXXX cannot be accessed.

- ***** PRIVILEGED INSTRUCTION TRAP *****
  LOCATION COUNTER : XXXX

- ***** SEGMENT TRAP *****
  LOCATION COUNTER : XXXX

- ***** NON MASKABLE INTERRUPT *****
  LOCATION COUNTER : XXXX
  STATUS/CONTROL REGISTER NOT READY
  LOCATION COUNTER : XXXX

  These messages are issued by the program when a system error occurs.

- **XXXX IS A BAD VECTOR**

  Issued during the special interrupt test when a different interrupt vector from the one expected is verified. XXXX is the detected vector.

- **NOT INTERRUPT**
  I HAVE TRIED WITH VECTOR XXXX

  This message is issued when the special interrupt is not verified. XXXX is the vector of the expected interrupt.

- **MESSAGE NOT ACKNOWLEDGED**

  This message is issued by the sending controller during the sending and receiving test when the message sent is not received by the target controller.

- **MESSAGE DATA FIELD TOO LONG**

  This message is issued by the sending controller during the sending and receiving test when the target controller receives a longer message than it has been programmed for.

- **INITIALIZED DESTINATION SOCKET**

  This message is issued by the sending controller during the sending and receiving test when the target controller has not been initialized.

- **INCORRECT MESSAGE CONT. FIELD LENGTH**

  This is issued by the sending controller during the sending and receiving test when an error in the control message is detected.

- **INVALID SOCKET NAME**

  Issued during the sending and receiving test when an invalid name is given for the target socket.

- **SOCKET IN USE**

  This message is issued during the sending and receiving test when an attempt is made to set a socket to receive while it is in use.

- **INCORRECT NODE NUMBER**

  Issued during the sending and receiving test when the sending controller is given an incorrect target node number while launching a transmit command.

- **WRONG SETUP RECEIVE (BOARD UNDER TEST)**

  This message is issued by the program when an error is detected while setting up the board under test to receive.

- **WRONG SETUP RECEIVE (ACTIVE LOOP)**

  This message is issued by the program when an error is detected while setting up the reference board to receive.

- **TX TIME-OUT (MASTER MACHINE)**

- **RX TIME-OUT (MASTER MACHINE)**

These messages are issued when there is a timeout on the board under test; the first is issued after a transmit command, and the second after a receive command.

- **TX TIME-OUT (SLAVE MACHINE)**

- **RX TIME-OUT (SLAVE MACHINE)**

These messages are issued when there is a timeout on the reference board; the first is issued after a transmit command, and the second after a receive command.

- **END OF TRANSMISSION (MASTER MACHINE)**

- **END OF RECEPTION (MASTER MACHINE)**

These messages are issued by the program when end of transmission and end of reception are respectively verified on the controller under test.

- **END OF TRASMISSION (SLAVE MACHINE)**

- **END OF RECEPTION (SLAVE MACHINE)**

These messages are issued by the program when end of transmission and end of reception are respectively verified on the reference controller.

- **UNATTENDED INTERRUPT**

This message is issued when an unexpected interrupt is verified during sending and receiving.

- **XXXX CHARACTERS TRANSMISSION**

This message is issued by the program every time a sending and receiving phase is initialized; XXXX can be 511, 1023, 1535 or 2043.

- **RETRY NUMBER XX**

Issued by the sending controller when several attempts to send are made before the message is received by the target controller; XX is the number of tries made.

- **UNRECOGNIZED ERROR**

This message is issued when an indication which is not in the range of possible errors is included in a send or receive command.

10.1 7032E5: FDU AND mFDU ERROR RATE PROGRAM

PROGRAM PURPOSE

To determine the error rate of the mFDU or FDU subsystem under simulated critical conditions.

HARDWARE REQUIRED

mFDU system or XU6030 (1MB) FDU with G0280/B-D controller, scratch disk (conforming to STANDARD 17 i.e. DF128/MFM256).

mFDU system:

PERIPHERAL	CONTROLLER
MFDU 320 KB (XU 4301)	G0280/C-E
MFDU 320 KB (XU 4350)	G0280/E
MFDU 1 MB (XU 4305)	G0280/B-D
MFDU 1 MB (ND08 DE)	G0280/D

NOTE

The controller cannot be inserted in slot 16 onwards as the program treats slot 16 as slot 0 and slot 17 as slot 1 and so on.

WARNING

The write operation in this program will overwrite on the program disk if left inserted. A scratch disk should therefore be substituted after loading the program. The disk is then identified and formatted automatically by the program.

LOADING PROCEDURE

Refer to section 1.3.2

10.1.1 TEST DESCRIPTION

All the tests except test 5 starts from be run in the order given by the default sequence or in a sequence selected by the operator. These tests are described below.

WRITE & VERIFY FORWARD (FROM OUTERMOST TO INNERMOST CYLINDER) - TEST 1

Writes a test pattern on a defined number of cylinders starting from the outermost cylinder and progressing towards the innermost cylinder and then verifies the the data written.

READ BACK (FROM INNERMOST TO OUTERMOST CYLINDER)- TEST 2

Reads a test pattern on a defined number of cylinders starting from the innermost cylinder and progressing towards the outermost cylinder and then verifies the data read.

WRITE & VERIFY BACK (FROM INNERMOST TO OUTERMOST CYLINDER)- TEST 3

The test is similar to TEST 1 except that data is written starting from the innermost cylinder and progressing towards the outermost cylinder.

READ FORWARD (FROM OUTERMOST TO INNERMOST CYLINDER)- TEST 4

The test is similar to TEST 2 except that data is read starting from the outermost cylinder progressing towards the innermost cylinder.

READ RANDOM - TEST 5

The test is similar to TEST 2 except that data is read using random addressing and random transfer lengths.

10.1.2 ERROR MESSAGES

If any of the following error messages are displayed check/change the HDU.

a) **CONFIGURATION/INITIALIZATION ERRORS**

- **PU ABSENT:**

  indicates that the peripheral is not connected to the controller.

- **PU NOT READY:**

  re-load the program if error persists or if the message appears during program execution the peripheral unit is considered faulty.

- **CONTROLLER INITIALIZATION ERROR:**

  re-load the program, if the fault persists attempt to re-load the program with another peripheral unit.

- **UNKNOWN PU TYPE SELECTED:**

  indicates that the peripheral name is not correct.

b) **ERRORS ORIGINATING FROM DISK**

- **TRACK 0 UNREADABLE! STD 17**
  NOT FOUND. PROGRAM ABORTS

- **STD 17 RECORDED ON TRACK 0 NOT CORRECT PROGRAM ABORTS**

c) **POSITIONING ERRORS**

- **HOME ERROR:**

  displayed when a HOME command fails.

- **SEEK ERROR:**

  displayed when a SEEK command fails.

- **WRONG CYLINDER SELECTED**
  EXPECTED CYL=XXX SELECTED CYL=YYY:

  displayed when the cylinder selected is recognised by the program but is NOT the expected cylinder.

- **WRONG CYLINDER SELECTED**
  EXPECTED CYL=XXX: SELECTED A BAD CYLINDER

  displayed when the cylinder selected is NOT the expected cylinder and is recognised by the program to be a bad cylinder.

- **UNKNOWN CYLINDER SELECTED**
  EXPECTED CYL=XXX

  displayed when the cylinder selected is recognised by the program.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO CYL= YYY:

  displayed when a cylinder positioning is lost during I/O operations and the program has stopped on cylinder YYY.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO BAD CYL:

  displayed when cylinder positioning is lost during I/O operations and the program has stopped on a bad cylinder.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO UNKNOWN CYL:

  displayed when cylinder positioning is lost during I/O operations and the program is NOT able to determine on which cylinder the

program has stopped.

- **SECTOR IDENTIFIER NOT FOUND**
  CYL=XXX SECT=ZZZ:

  displayed once only when the identifier of a sector is NOT recognised or is illegible or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected (i.e. set to 1).

- **DATA FIELD NOT FOUND**
  CYL=XXX SECT=ZZZ:

  indicates that the synchronization characters preceding the data of a sector are NOT recognised; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected.

d) **WRITE ERRORS**

- **CANNOT WRITE HISTORY TRACK**
  PROGRAM ABORTS

- **DATA FIELD WRITE ERROR**
  CYL: XXX SECT: ZZZ

  indicates an error on a sector during a WRITE operation; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected.

- **ERROR ON CYL: XXX YY SECT: ZZZ**
  WRITE NUMBER: UUUUUU
  DATA FIELD ERRORS N: VVVVVV
  DATA MARK NOT FOUND N: WWWWWW
  SECTOR NOT FOUND N: @@@@@@
  ERROR RATE: ID= > OR < xx% DATA= > OR < yy%
  MAX CONSECUTIVE ID OR DATA ERR: zzzzz:

  displayed if a WRITE operation on a sector fails; note that the result of the error rate calculations are given together with the address of the faulty sector and that any non-significant field is indicated with "?" (xx/yy= threshold value entered by the operator)

e) **READ ERRORS**

- **CANNOT READ HISTORY TRACK**

  program aborts

- **DATA FIELD READ ERROR**
  CYL: XXX SECT: ZZZ
  BURST LENGTH: xxx
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy:

indicates that a READ error on a sector is recovered by ECC; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected; note that the sector address, burst length, write pattern, read pattern and displacement characters (from the start of the sector to the first incorrect character) are indicated.

- **ERROR ON CYL: XXX SECT: ZZZ**
  READ NUMBER: UUUUUU
  DATA FIELD ERRORS N: VVVVVV
  DATA MARK NOT FOUND: vvvvvvv
  BURST LENGTH
  MAX: mmm MIN: nnn
  SECTOR NOT FOUND N: aaaaaa
  ERROR RATE: ID= > OR < xx% DATA= > OR < yy%
  MAX CONSECUTIVE ID OR DATA ERR: zzzzz:

  displayed if a READ operation on a sector fails; note that the result of the error rate calculations are given together with the address of the faulty sector and other relevant parameters; any non-significant field is indicated with "?" (xx/yy= threshold value entered by the operator).

f) **HARWARE ERRORS**

The following messages are self explanatory and are displayed as the result of the hardware error counter threshold value being exceeded.

- **INCOHERENT I/O ROUTINE ANSWER**
  HARDWARE ERROR

- **MEMORY TRANSFER DATA NOT DETECTED**
  BY THE SYSTEM. HARDWARE FAILURE
  CYL: XXX SECT: ZZZ
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy

- **TIME OUT DURING I/O OPERATION**
  HARDWARE FAILURE

- **HARDWARE FAILURE**

  indicates general hardware failure.

- **PU HARDWARE FAILURE**

  indicates peripheral unit (disk) hardware failure.

10.2 MFDMA1: FDU DRIVER ALIGNMENT AND ECCENTRICITY CHECK

PROGRAM PURPOSE

To check alignment of the heads and eccentricity of the spindle of the floppy disk subsystem, ensuring that the unit is operating within the accepted tolerances.

HARDWARE REQUIRED

The TECHMOST DAT52/N double side MFM256 testing tool and one of the following mFDU systems:

PERIPHERAL	CONTROLLER
MFDU 320 KB (XU 4301)	G0280/C-E
MFDU 320 KB (XU 4350)	G0280/E
MFDU 1 MB (XU 4305)	G0280/B-D
MFDU 1 MB (ND08 DE)	G0280/D

WARNING
The program should NOT be used as a means of regulating the minifloppy subsystem.

LOADING PROCEDURE

Refer to section 1.3.2

10.2.1 TEST DESCRIPTION

ALIGNMENT MEASUREMENT

Alignment is measured by checking that track 16 has been read correctly and then making a comparison test with the number of tracks legible inside track 16 and the number of tracks legible outside track 16.

ECCENTRICITY MEASUREMENT

The degree of eccentricity, is calculated using algorithms and the result is shown in a summary table at the end of the program.

10.2.2 ERROR AND SERVICE MESSAGES

error messages marked ** can be put right by the operator ie "pu not ready". The majority of the errors refer to the floppy disk unit, therefore if an error occurs change this first.

- Marginated disk not recognized!

- Too large alignment value!
  A rough calibration is necessary if you want to continue
  Calibrate and hit <ENTER> to retry or hit <SKIP> to end program **

- Incoherent counter format (non-blocking error)
- OVERFLOW!! (non-blocking error)
- Write error during counter updating (non-blocking error)
- No track with all readable sectors
- Warning! only # tracks read on side 0/1 (less than 14 tracks read)
- Internal Alignment out of tolerance
- External Alignment out of tolerance
- Eccentricity value out of tolerance
- Eccent. + Align. out of tolerance
- hardware error
- hardware fault
- f.d.c busy (f.d.c. = floppy disk controller) **
- hardware fault recovered
- operator interference! **
- unknown controller **
- unknown interrupt
- incoherent answer
- motor ignition fault
- incoherent status
- pu not ready **
- write protect **
- Time out error

10.3 FDUMA2: FDU DRIVER ALIGNMENT AND ECCENTRICITY CHECK PROGRAM

PROGRAM PURPOSE

To check alignment of the heads and eccentricity of the spindle of the floppy disk subsystem, ensuring that the unit is operating within the accepted tolerances.

HARDWARE REQUIRED

XG6030 (1MB) FDU, G0280/B-D controller and one of the following TECNOST media: i) DAT82 DOUBLE SIDE FDU TESTING TOOL MFM256 or ii) FDU DOUBLE FACE TEST DISK DF128.

WARNING

The program must NOT be used as a means of calibrating the floppy disk subsystem.

LOADING PROCEDURE

Refer to section 1.3.2

10.3.1 TEST DESCRIPTION

ALIGNMENT MEASUREMENT

Alignment is measured by checking that track 36 has been read correctly and then making a comparison test with the number of tracks legible inside track 36 and the number of tracks legible outside track 36.

ECCENTRICITY MEASUREMENT

The degree of eccentricity, is calculated using algorithms and the result is shown in a summary table at the end of the program.

10.3.2 ERROR AND SERVICE MESSAGES

Refer to the MFDMA1 program section 10.2.2 for the relative error and service messages.

10.4 4301T4: XU4301 PERIPHERAL TEST PROGRAM

PROGRAM PURPOSE

To test the mFDU by running a number of tests which require use of the test disk and, in certain cases, a scratch disk.

HARDWARE REQUIRED

XU4301 mFDU (320KB), G0280/C-E controller and a 320KB scratch disk which comforms to Standard 17 (DF128 or MFM256).

PRELIMINARY WARNING

The write test of this program modifies the entire data field.

The write tests are performed also on the alternative tracks of the floppy disk. These tracks must not, therefore, have been allocated or the disk will be rejected by the program.

The controller must only be in slots 1-12

LOADING PROCEDURE

Refer to section 1.3.2

10.4.1 TEST DESCRIPTION

1) CONTROLLER COMMUNICATION TEST

The communication channel is tested, the controller is initialised, its type is ascertained and displayed.

2) TIMER TEST

Interrupts and controller internal DMA requests are disabled and the timer test run. The interrupts and controller internal DMA requests are then re-enabled.

3) INTERRUPT TEST

The interrupt and internal DMA transfer networks are disabled, the static test is run on the interrupt network, and the DMA and interrupt network are re-enabled. The vectored interrupts are then tested with the controller re-initialized (using the timer).

4) DMA TEST

The internal DMA and interrupt network are disabled, a static test is run on the DMA network, a dynamic test is run on DMA addressing with simulated transfers to memory, and finally the internal DMA and interrupt network are re-enabled.

5) COMPATIBILITY TEST

The controller is initialized and the type of disk checked. The disk formatting is then checked to ensure that there are no defective tracks and also a check made to see if there is a write protect condition. The disk characteristics are displayed.

6) SPEED MEASUREMENT TEST

The minimum, maximum and average rotation time of the disk is measured and compared with nominal values. An histogram of speed measurements is then displayed.

7) SEEK TEST

Checks the positioning of the head on tracks 1 to 37. After each SEEK command there is a HOME command.

8) FORMAT TEST

A track is formatted and checked to see if it has been correctly formatted. The track is then erased and the operation repeated.

9) READ TEST

A read operation is made on a cylinder and track selected randomly using transfers of various lengths. Then the operation is repeated on a different cylinder and head and the data read compared.

10) WRITE & READ SECTOR TEST

Data is written on all the sectors of the last physical cylinder then the data is read and compared with the original data in memory.

11) WRITE & READ DELETED TEST

Data is written on all deleted sectors on two alternative cylinders then the data is read and compared with the original data in memory.

12) CONTROL MARK TEST

Three sectors are recorded alternatively "normal", "deleted" and "skip deleted". The sectors are then recorded "deleted", "normal", "deleted" and "skip normal". Finally, the entire physical track is read and checked.

13) WRITE & READ CYLINDER TEST

The write/verify/read command cycle on a track is checked, comparing the data read with data in memory. The program also checks for the presence of deleted sectors on the two alternative sectors.

10.4.2 ERROR MESSAGES

Fault finding notes:

- Errors found in tests 1 to 4, 11 and 12 verify/change the controller board.
- Errors found in test 5 verify/change the disk
- Errors found in test 6 verify/change the disk unit
- Errors found in test 7 verify/change in the following order: the disk, the controller and/or the disk unit
- Errors found in test 7 verify/change in the following order: the controller and/or the disk unit

List of error messages:

- INCOHERENT STATUS (controller response not recognised)
- NOT PROVIDED CONTROLLER TYPE: WAITED **** RECEIVED **** (the controller connected is not the one expected)
- INVALID COMMAND (not recognised by controller)
- HARDWARE FAULT
- CHANNEL BUSY (an earlier command is still pending)
- COMMAND ABORTED FOR P.U. NOT READY
- FDC CHARACTER EXCHANGE ERROR (exchange error between CPU and FDC)
- COMMAND ABORT FOR T.O. (end of time out command)
- PU ABSENT (peripheral unit absent)
- INDEX PULSES NOT RECEIVED (in cycle time measurement)
- TIMEOUT ERROR (software)
- INTERRUPT CODE INCOHERENCE : CODE EXPECTED ** RECEIVED **
- INTERRUPT IDENTIFIER INCOHERENCE : CODE EXPECTED ** RECEIVED **
- TIME ERROR : CHANNEL 0 FAULT (error traced to channel 0)
- DMA CONTROLLER ERROR:
  TRANSFER NOT TERMINATED
  TRANSFER NOT CORRECT
  CHANNEL 1 FAULT
  CHANNEL 2 FAULT
- INTERRUPT NOT RECEIVED

- TIMEOUT INTERRUPT NETWORK FAULT
- TIMER INTERRUPT NETWORK FAULT
- FDC INTERRUPT NETWORK FAULT
- PARITY ERROR INTERRUPT FAULT
- DMAC INTERRUPT NETWORK FAULT
- INOP DETECTED ON INIT X : INOP DETECTED (response to first command after door has been opened)
- MOTOR IGNITION FAULT (motor start not available)
- PU NOT READY (peripheral not ready)
- EDC ERROR IN DATA FIELD
- EDC ERROR IN IDENTIFIER FIELD
- DMA OVERRUN
- DMA TRANSFER NOT COMPLETED : $$$$ BYTE TRANSFERRED INSTEAD OF $$$$
- UNEXPECTED "DELETED" SECTOR(S) FOUND
- UNEXPECTED "NORMAL" SECTOR(S) FOUND
- BAD FORMATTING ON CYL: $$
- BAD DELETING ON CYL: $$
- DATA COMPARISON INCOHERENCE
- POSITIONING ERROR
  START CYL: $$
  END CYL: $$
  FOUND CYL: $$
  UNKNOWN HD POSITION
- MISSING SIGNAL OF WRONG CYL
  HEAD POSITIONED ON CYL $$
  READ COMMAND MADE ON CYL $$
- WRONG SECTOR
- CYL:$$ SECT:$$ (to show position of head)

10.5 4305T6: PERIPHERAL UNIT XU4305 TEST PROGRAM

PROGRAM PURPOSE

To test the mFDU by running a number of tests which require use of the test disk and, in certain cases, a scratch disk.

HARDWARE REQUIRED

XU4305 mFDU (1MB), G0280/B-D controller, scratch disk (1 MB) conforming to standard 20.

PRELIMINARY WARNING

The write test of this program modifies the entire data field.

The write tests are performed only on the alternative tracks of the floppy. These tracks must not, therefore, have been allocated or the disk will be rejected by the program.

The controller must only be in slots 1-12

LOADING PROCEDURE

Refer to section 1.3.2

10.5.1 TEST DESCRIPTION

See corresponding sections of the 4301T4 program for test description (sect. 10.4.1) and list of error messages (sect. 10.4.2).

10.6 6030T6: XU6030 PERIPHERAL TEST PROGRAM

PROGRAM PURPOSE

To test the FDU by running a number of test which require use of the test disk and, in certain cases, a scratch disk.

HARDWARE REQUIRED

XG6030 FDU (1MB), G0280/B-D controller, scratch disk (1 MB) conforming to Standard 20 (DF128 or MFM256).

WARNING

The write test of this program modifies the entire data field.

The write tests are performed only on the alternative tracks of the floppy. For this reason, these tracks must not have been allocated or the disk will be rejected.

The controller must only be in slots 1-12

LOADING PROCEDURE

Refer to section 1.3.2

10.6.1 TEST DESCRIPTION

See corresponding sections of the 4301T4 program for test description (sect. 10.4.1) and list of error messages (sect. 10.4.2).

11.1 505CT9: STC TO XU 5010 SAVE/RESTORE PROGRAM (VIA HDU CONTROLLER)

PROGRAM PURPOSE

To test the HDU and STC and in particular to evaluate the error rate of data transfers in which both the STC and HDU are operated in overlapped mode.

HARDWARE REQUIRED

RAM board (384 Kb min.), XU51010 HDU with G0230 and G0231 controller boards, STC system as follows:

PERIPHERAL	CONTROLLER
XU1120 STC	G0200/B & G0201/B
XU1130 STC cartridge tape	G0200/B & G0342

WARNING

In write, save and restore operations, data on both tape and disk are destroyed.

To avoid losing data transfers should, therefore, be limited to those sectors and tracks which do not have valuable data.

NOTE

Test sequence must be carried out in the following order:

8) ERASE TAPE;	OR	8) ERASE TAPE;
3) WRITE TAPE;		1) WRITE HDU;
6) TAPE ---->HDU;		5) HDU ---->TAPE;
2) READ HDU		4) READ TAPE

OPERATING PROCEDURE

Refer to section 1.3.2.

11.1.1 TEST DESCRIPTION

1) ? WRITE HDU

An incrementing pattern, from %0000 to %7FFF, is written on the sectors of the disk specified in the pre-program.

2) ? READ HDU

The disk is read and the data read compared with the test pattern in memory.

3) * WRITE TAPE

A decrementing pattern, from %FFFF to %8000, is written on the tracks of the tape specified in the pre-program.

4) ? READ TAPE

The tape is read and the contents compared with the test patterns in memory.

5) * HDU --> TAPE

A SAVE operation is carried out, i.e. the contents of the disk are transferred to the tape.

6) ? TAPE --> HDU

A RESTORE operation is carried out, i.e. the contents of the tape are transferred to the disk.

7) ? PRECOND TAPE

The tape is wound through to the end and then rewound back to the beginning, thus ensuring it is sufficiently taut.

PRECOND COMPLETED: TIME MM'SS''
indicating the end of the operation and the time taken.

8) ? ERASE TAPE

The area of tape specified in the pre-program is erased.

9) ? REWIND TAPE

The tape is rewound completely.

10) ? PAUSE

A pause interval as in the pre-program is obtained.

11.1.2 ERROR AND SUMMARY MESSAGES

If any of the following error messages are indicated try changing the peripheral unit indicated (HDU or STC) then if fault persists change the associated controller.

All error messages relating to the HDU subsystem are preceded by:

HDU ERROR DETECTED:

The HDU error messages are:

PU IN PERMANENT FAILURE

PU IN TRANSITORY FAILURE

PU NOT READY

HARDWARE ERROR

TIMEOUT ERROR: INTERRUPT NOT RECEIVED

SYSTEM BUS ERROR

ERROR DURING WRITE OPERATION

PU NOT KNOWN

PU ABSENT OR DOES NOT ACKNOWLEDGE

ERROR DURING READING PHASE

ERROR DURING WRITING PHASE

IDENTIFIER ERROR:
ID. SOUGHT.:FB=%XX CY=CC HD=H ST=SS
ID FOUND :FB=%XX CY=CC HD=H ST=SS
DATA ERROR:
FB=%XX CY=CC HD=H ST=SS
ECC ERROR:
FB=%XX CY=CC HD=H ST=SS

All STC error messages are preceded by:

TAPE ERROR DETECTED:

The STC error messages are listed below:

HARDWARE ERROR

CARTRIDGE NOT INSERTED

STC BUSY

PERMISSION DENIED: WRITE PROTECT

INTERRUPTION BY OPERATOR

ADDRESS NOT ALIGNED

MEMORY TRANSFER FAULT

ERROR DURING WRITE: CARTRIDGE CRASH

ERROR DURING READ: CARTRIDGE CRASH

UNEXPECTED EOT

ONE BUFFER NOT TRANSFERRED

WRITE ATTEMPTED ON NOT ERASED TRACK

MAIN MEMORY DATA COMPARE ERROR

(HARDWARE NOT RELIABLE)

ALL DATA NOT TRANSFERRED

SOME DATA NOT TRANSFERRED

WRONG DATA TRANSFERRED

WRONG BLOCK LABEL FOUND

SUMMARY MESSAGES

At the end of the program, a table summarising the results of all tests performed is displayed:

```
--- TAPE TRANSFER SUMMARY ---
=========================================
|READ BLOCKS:                |    AA     |
|OPERATION(S) WITH REPET.:   |    BB     |
|REPEATED BLOCK(S)           |    CC     |
+-------------------------------------------+
|WRITTEN BLOCKS:             |    DD     |
|OPERATION(S) WITH REPET.:   |    EE     |
|REPEATED BLOCK(S):          |    FF     |
+-------------------------------------------+
|COMPARE ERROR(S)            |    GG     |
=========================================

--- HDU TRANSFER SUMMARY ---
=========================================
|READ SECTORS:               |    HH     |
|ERROR(S) DETECTED:          |    II     |
+-------------------------------------------+
|WRITTEN SECTORS:            |    LL     |
|ERROR(S) DETECTED:          |    MM     |
+-------------------------------------------+
|COMPARE ERROR(S)            |    NN     |
=========================================
```

Where:

- AA = no. blocks read (in tape read operation)
- BB = no. operations with repeated blocks (in tape read)
- CC = no. blocks repeated (in tape read)
- DD = no. blocks written (in tape write)
- EE = no. operations with repeated blocks (in tape write)
- FF = no. blocks repeated (in tape write)
- GG = no. errors found in data compare after tape write
- HH = no. sectors read
- II = no. errors found in disk read
- LL = no. sectors written
- MM = no. errors found in disk write
- NN = no. errors found in data compare after disk write

11.2 HDSCPH: DUMP-RESTORE FROM HDU TO STC AND VICEVERSA - FOR ETS WS

11.2.1 PROGRAM PURPOSE

To test the HDU and STC in dump/restore operations.

11.2.2 HARDWARE REQUIRED

HDU system and STC systems.

HDU systems:

HDU	CONTROLLER
OPE 18MB (XU5010)	5010 INT. (G0230 andG0231)

Other systems:

PERIPHERAL	CONTROLLER
STC (XU1120)	G0200/X or B and G0201/B

NOTE

The program must only be used in ETS2030/2034/2040/2044/2060.

The program transfers only the operative system and DCOS from HDC to STC and vice-versa.

WARNING

The program also destroys any data stored on the HDU or STC.

11.2.3 OPERATING PROCEDURES

Refer to section 1.3.2.

11.2.4 TEST DESCRIPTION

The program makes a physical transfer of the operative system from the HDU to STC and vice-versa and then makes a comparison test with original data to see if there are any discrepancies.

11.2.5 ERROR MESSAGES

If there are errors try changing the appropriate peripheral unit (HDU or STC) and/or associated controller as indicated by the error message unless otherwise indicated.

a) **SLOT TEST**

The program initially checks if the controllers are in their correct slots. If there are errors one of the following messages is displayed:

- THE PRESENT CONTROLLER IN SLOT XX ANSWER PHYSICAL NAME YY INSTEAD OF ZZ
- STC MISSING
- THE SLOT IS EITHER EMPTY OR CONTAINS A NON SELF-DECLARING CONTROLLER

b) **STC WRITE PHASE (HDU to STC i.e. DUMP)**

If an error is found during this phase the program attempts a recovery operation. If more than 20 blocks per track are recovered the operations are trunkated and the following error messages is displayed.

- ERROR ON WRITE : CARTRIDGE CRASH

c) **SAVE VERIFY PHASE (DUMP AND VERIFY)**

If errors are found during the verify phase (i.e. between reference data and data read) the following error message is displayed and the position of the first incorrect character is indicated together with the successive 16 characters read and the corresponding reference characters:

- ERROR ON READ: CARTRIDGE CRASH

d) **WRITE HDU PHASE (STC to HDU - RESTORE)**

Errors found during this phase are usually in the data field verify operation or in the registration and verification positioning operation.

In this case the cylinder, head and sector on which the error was found is displayed and a verify operation is performed on the successive sectors.

Note that if the error is on the last sector of a track the verify operation is continued on the next track.

e) **RESTORE VERIFY PHASE**

Typical errors are found:

- in positioning operations during read phase,
- in data field,
- in comparison test.

f) **CARTRIDGE NOT INSERTED**

Displayed if cartidge is not correctly inserted.

11.3 SCT303: G0200B/G0201B BOARDS (STC CONTROLLER) TEST PROGRAM

PROGRAM PURPOSE

To test and diagnose the STC subsystem, consisting of two printed circuit boards and a magnetic tape peripheral unit.

HARDWARE REQUIRED

STC controller boards (G0200B/G0201B), Streaming Cartridge Tape unit (XU1120).

WARNING

This program is valid only with firmware release 7.0 and subsequent releases, as only these releases have the appropriate diagnostic commands.

OPERATING PROCEDURE

Refer to section 1.3.2.

11.3.1 TEST DESCRIPTION

As tests 10, 11 and 12 (REWIND, PRECONDITIONING TAPE and ERASE TEST) are run in connection with other tests (see description below), they should only be run by themselves where necessary.

1) CHECK AFTER AUTODIAGNOSTIC TEST

This test checks out the status of the controller after the autodiagnostic test and after a Software Reset.

2) CHECK COMMAND AND STATUS PORT TEST

This is the Olibus communication port (Command/Status Port) diagnostic test, performed by writing data on the command port and issuing the STATUS PORT TEST firmware command by way of which the data written on the Command Port is read on the Status Port.

3) READ/WRITE VECTOR INTERRUPTS TEST

This is the interrupt port diagnostic test. A certain number of vectors are written on the command port and the LOAD INTERRUPT VECTOR TEST firmware command, by way of which the vector and the control character are written, then issued.

4) READ DATA IN MAIN MEMORY TEST

This test checks the controller's ability to address and read system memory.
A 16 byte buffer is complied and the READ SYSTEM MEMORY TEST firmware command issued. This command compares the data read by the system with the pattern received when the command is issued.

5) WRITE DATA IN MAIN MEMORY TEST

The controller's ability to address and write system memory is tested. The firmware command WRITE SYSTEM MEMORY TEST is issued in which a 16 byte record is compiled in system memory with the pattern received when the command is issued.

6) LOAD/STORE IN MAIN MEMORY TEST

This tests the controller's ability to perform data exchanges between system memory and local RAM (Software DMA). The LOAD RAM firmware command is issued in which the record read in system memory is compiled in local storage. The STORE RAM firmware command is then issued to transfer part of the contents of local RAM into system memory.

7) MEM/MEM DMA CONTROLLER TEST

In this test, a buffer is exchanged between two areas of local memory by way of the DMA CONTROLLER 8237A. The LOAD RAM firmware command is issued, transferring into RAM a program written in Z8002 language. The RUN PROGRAM firmware command is then issued to execute the program previously loaded.

8) WRITE/READ ONE DATA BLOCK ON TRACK 0

This test implements the I/O WRITE/READ routines. A command specifying a data block write on tape track 0 is sent out to the peripheral; this block is subsequently read and compared with the original block written. The status of both the controller and the peripheral unit are checked following issue of each command. At the start of the test, the tape is rewound and approx. 3 meters of tape is erased.

9) WRITE/READ DATA BLOCK ON ALL TRACKS

This test involves use of the I/O WRITE/READ routines. A command specifying a data block write on the 4 tracks of the tape is issued; the data block is subsequently read and compared with the block written originally. The status of both the controller and the peripheral unit are checked following issue of each command. Before the test starts, the tape is rewound and erased completely.

10) REWIND TEST

The I/O REWIND routine is used in this test. The tape rewind command is sent out to the peripheral unit. Controller status and peripheral unit status are checked at the end of the command.

11) PRECONDITIONING TAPE TEST

The tape tension command is sent to the peripheral unit in this test by way of the PRECONDITIONING I/O routine. Controller status and peripheral unit status are checked at the end of the command.

12) ERASE TAPE TEST

In this test, the erase all tape tracks command is sent to the peripheral unit by way of the I/O routine ERASE. Controller status and peripheral unit status are checked at the end of the command.

11.3.2 ERROR MESSAGES

In case of errors try resetting the system and repeat tests. If fault persists try changing/checking the controller boards (HDU boards first) then the peripheral units (unless otherwise indicated).

- ***** PRIVILEGED INSTRUCTION TRAP *****
- ***** SEGMENT TRAP *****
- ***** NON MASKABLE INTERRUPT *****
- **INCOHERENT MESSAGE REPEAT ALL TESTS**
- **ERR. CONTROLLER AFTER RESET**

Error messages pertaining to test 1

- **INCOERENT MESSAGE REPEAT ALL TESTS**
- **ERR. DAB00/DAB07 ON LDE9 F.L.05 D13**
- **ERR. SBUS0 = 1 BEFORE START COMMAND**
- **ERR. SBUS0 = 0 DURING COMMAND**
- **ERR. SBUS0 = 1 AFTER START COMMAND**
- **ERR. EPROM IN AUTODIAGNOSTIC TEST**
- **ERR. RAM IN AUTODIAGNOSTIC TEST**
- **ERR. DMA.CONTR. IN AUTODIAGNOSTIC TEST**

- ERR. CPU Z8002 OR INTERN BUS

Error messages pertaining to test 2

- ERR. AFTER START CHECK STATUS COMMAND
- ERR. CHECK STATUS COMMAND END
- ERR. AFTER WRITING DATA ON COMMAND PORT
- ERR. F.L.05 DA000/70 N13 DAB09/15 L13

Error messages pertaining to test 3

- ERR. AFTER START LOAD INTERRUPT COMMAND
- ERR. AFTER WRITING INTERRUPT VECTOR
- ERR. LOAD INTERRUPT COMMAND END
- VERIFY SIGNALS WRINN TO VINTA F.L:05
- ERR. F.L:05 DA000/70 D11 DAB00/07 D13

Error messages pertaining to test 4

- ERR. AFTER COMMAND STARTED
- ERR. AFTER WRITE ADDRESS HIGHT
- ERR. AFTER WRITE ADDRESS MIDDLE
- ERR. AFTER WRITE ADDRESS LOW
- ERR. READ IN MAIN MEMORY COMMAND END
- ERR. GOMEN =1 VERIFY LEDA0 =0 GOLOA =1
- ERR. F.L.02 VERIFY BD000/150 ALS01/11

Error messages pertaining to test 5

Identical to the test 4 error messages.

Error messages pertaining to test 6

- INCOERENT MESSAGE REPEAT ALL TESTS
- ERR. CONTROLLER AFTER RESET
- ERR. AFTER LOAD RAM COMMAND STARTED
- ERR. AFTER WRITE ADDRESS HIGHT
- ERR. AFTER WRITE ADDRESS MIDDLE

- ERR. AFTER WRITE ADDRESS LOW
- ERR. AFTER WRITE ADDRESS LOCAL RAM
- ERR. AFTER WRITE LENGTH BUFFER
- ERR. AT LOAD RAM COMMAND END
- ERR. AFTER STORE RAM COMMAND STARTED
- ERR. AT STORE RAM COMMAND END
- ERR. F.L.02 AD500/15 BD000/150 A06/C06

Error messages pertaining to test 7

Identical to the test 6 error messages with the following additional messages:

- ERR. AFTER EXECUTE RAM COMMAND STARTED
- ERR. AFTER WRITE ADDRESS LOCAL RAM
- ERR. BD000/70 AL509/15 F.L.03 B03

Error messages pertaining to test 8

Identical to the test 6 error messages.

Error messages pertaining to tests 9, 10, 11 and 12.

- ERR. RESET COMMAND END
- ERR. AFTER LOAD INTERRUPT COMMAND STARTED/END
- ERR. AFTER INITIALIZATION COMMAND STARTED
- ERR. CONTROLLER NOT READY
- ERR. ADDRESSING MMCA REPEAT ALL TESTS
- ERR. AFTER COMMAND STARTED
- INCOHERENT ANSWER AFTER COMMAND
- INCOHERENT ANSWER FROM I/O ROUT. STATUS
- BB CONTROLLER NOT INITIALIZATING
- ERR. C1N00 =1 NOT INSERTED CARTRIDGE
- ERR. SAFE0 =0 CARTRIDGE WRITE PROTECT
- ERR. AFTER SEARCH COMMAND STARTED

- INCOHERENT ANSWER AFTER SEARCH COMMAND
- CC CONTROLLER NOT INITIALIZATING
- ADDRESS NOT ALIGNED VERIFY ADDRESS BUS
- INCOHERENT ANSWER AFTER READ COMMAND
- ERR. BD000/70 ALS09/15 F.L.03 B03
- ERR. AFTER WRITE COMMAND STARTED
- INCOHERENT ANSWER AFTER WRITE COMMAND
- EE CONTROLLER NOT INITIALIZATING
- ERR. AFTER STOP COMMAND STARTED
- INCOHERENT ANSWER AFTER STOP COMMAND
- FF CONTROLLER NOT INITIALIZATING

Other messages

- ERR. GOMEN =1 ERROR ON OLIBUS
- ERR. ORERN =0 READ ON ERROR
- ERR. LHTAP =1 LOW HOLE
- ERR. ERTRN =0 READ ON ERROR
- ERR. FDASO =1 CHECKING DATA FASE
- ERR. BUALO =1 HIGH HOLE FOUND
- ERR. BUALO =0 HIGH HOLE NOT FOUND
- ERR. EOPRN TO RIVEN ON PROCESSOR
- ERR. DMA CONTROLLER ADDRESSING CHANNEL 1/0
- ERR. DMA CONTROLLER COUNTER CHANNEL 1/0
- ERR. DMA CONTROLLER PENDENT REQUESTS

11.4 STC404: G0200B & G0342 DIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To evaluate the STC subsystem under critical operating conditions using read, write and append operations and also to test the service functions such as erase, rewind and preconditioning.

HARDWARE REQUIRED

RAM board (min. 256 KB), STC controller boards (G0 200B and G0342), Streaming Tape Cartridge unit (XU 1130) and tape.

NOTE:

1. The program can be run only on STC controllers with firmware releases no earlier than 8.0.

2. Program execution time using the recommended default sequence is 6 minutes if no errors are incurred.

WARNING

This program includes tape write operations so the operator should first ensure that data on the tape can be destroyed.

OPERATING PROCEDURE

Refer to section 1.3.2.

11.4.1 TEST DESCRIPTION

GENERAL

Tests 1, 2 and 3 concern the G0200B controller and can be run without the controller/formatter(G0342) connection. Refer to the same test headings, section 11.3.1 of the STC303 program for description.

Test 4 - NON MASKABLE INTER. GENERATION TEST checks the controller's ability to detect and indicate an error on the OLIBUS after a write operation has been initiated to an address reserved for the PROM.

Tests 5 through to 8 concern the controller and the formatter, refer to test 4 through to 7 respectively of section 11.3.1 of the STC303 program.

Tests 9 through to 14 are functional tests and must be run with the controller/formatter/driver connected. Refer to tests 8 through to 12 respectively of section 11.3.1 of the STC303 program for the corresponding test description.

11.4.2 ERROR MESSAGES

The error messages are the same as those shown in section 11.3.2 of the STC303 program with the exception of the G0202/B originated messages and the addition of the following messages:

- **ERR. AFTER READ DATA COMMAND STARTED**
- **ERR. AFTER WRITE DATA COMMAND STARTED**
- **CONTROLLER BUSY REFUSE COMMAND**
- **ERR. ERMEN =0 ERROR ON OLIBUS**

Try resetting the system and if fault persists verify/change the controller boards before replacing the STC unit.

The following are messages associated with the G0342 board (try changing the boards or tape to rectify error):

- **ERR. CAIN1 =0 NOT INSERTED CARTRIDGE**
- **ERR. USAF1 =0 CARTRIDGE WRITE PROTECT**
- **ERR. SEDR1 =1 TAPE SELECT**
- **ERR. SEDR1 =0 TAPE NOT SELECT**
- **ERR. LTAP1 =1 LOW HOLE FOUND**
- **ERR. LTAP1 =0 LOW HOLE NOT FOUND**
- **ERR. UTAP1 =1 HIGH HOLE FOUND**
- **ERR. UTAP1 =0 HIGH HOLE NOT FOUND**
- **MOTION ERROR**
- **ERR. SIGNAL TACH1 ABSENT**
- **ERR. PERIOD SIGNAL TACH1**
- **ERR. DATA READ DIFFERENT FROM %AA55**
- **ERR. MOERN =1 SINGLE READ ERROR**
- **ERR. MOERN =0 A LOT READ ERRORS**
- **ERR. ON SWITCHES UP TYPE TIPON/TIP3N**

11.5 SCTER7: STC SUBSYSTEM ERROR RATE EVALUATION PROGRAM

PROGRAM PURPOSE

To evaluate the STC subsystem error rate under critical operating conditions.

HARDWARE REQUIRED

RAM board (min. 256 KB), STC system comprising:

PERIPHERAL	CONTROLLER
XU1120	G0200/B and G0201/B
XU1130	G0200/B and G0342

WARNING

This program includes tape write operations so the operator should first ensure that data on the tape can be destroyed.

OPERATING PROCEDURE

Refer to section 1.3.2.

11.5.1 TEST DESCRIPTION

1) ? REWIND

The I/O routine to command tape rewind is issued.

A time-out is set to ensure that the tape is rewound in the time allowed.

At the same time as the time-out is set, a clock timer starts to record the time elapsed from the start of the test. At the end of the test, it shows the total time taken.

2) ? ERASE

The area of tape specified in the pre-program is erased.

3) ? PRECONDITIONING

The tape is wound through to the end and then back to the beginning to ensure it is sufficiently taut.

4) * WRITE

The pattern selected in the pre-program is written on the tracks specified in the pre-program.

5) ? READ

The tracks selected in the pre-program are read in streaming mode. The operator selects the number of blocks to be read at a time.

6) * APPEND

The blocks are appended a number of times to the track selected as specified in the pre-program.

A TAPE MARK is used to mark the end of the operation.

7) PAUSE

A pause time is introduced, the duration of which is established in the pre-program.

The following service messages are then displayed:

11.5.2 ERROR AND SUMMARY MESSAGES

Before replacing the STC unit verify/replace the controller boards (unless otherwise indicated).

HARDWARE ERROR

CARTRIDGE NOT INSERTED

STC BUSY

PERMISSION DENIED:
CARTRIDGE IN WRITE PROTECT MODE

INTERRUPTION BY OPERATOR

TIMEOUT OCCURRED

ADDRESS NOT ALIGNED

MEMORY TRANSFER FAULT

ERROR DURING WRITE: CARTRIDGE CRASH

ERROR DURING READ: CARTRIDGE CRASH

UNEXPECTED EOT ENCOUNTERED

ONE BUFFER NOT TRANSFERRED

WRITE ATTEMPTED ON TRACK NOT ERASED

APPEND DENIED ON THIS TAPE

READ ERROR COUNT OVERFLOW

WRITE ERROR COUNT OVERFLOW

APPEND ERROR COUNT OVERFLOW

ERROR LIMIT OVERFLOW

PROGRAM ABORT

MAIN MEMORY DATA COMPARE ERROR
HARDWARE NOT RELIABLE

TRACK IDENTIFIER WRONG

BLOCK IDENTIFIER WRONG

COMPARE ERROR COUNT OVERFLOW

SUMMARY MESSAGES

When the test program has been completed, a table is displayed in which all the messages summarizing the test results are found:

--- TAPE TRANSFER SUMMARY ---
TRACK TT (ALL TRACKS)

READ BLOCKS:	AA
OPERATION(S) WITH REPET.:	BB
REPEATED BLOCK(S)	CC
WRITTEN BLOCKS:	DD
OPERATION(S) WITH REPET.:	EE
REPEATED BLOCK(S):	FF
APPEND BLOCKS:	GG
OPERATION(S) WITH REPET.:	HH
REPEATED BLOCK(S)	JJ
COMPARE ERROR(S)	KK

where:

- TT = track summary refers to
- ALL TRACKS = if summary refers to all the tracks
- AA = no. blocks read (in tape read)
- BB = no. operations with repeated blocks (in tape read)

- CC = no. blocks repeated (in tape read)
- DD = no. blocks written (in tape write)
- EE = no. operations with repeated blocks (in tape write)
- FF = no. blocks repeated (in tape write)
- GG = no. of blocks appended
- HH = no. of operations with repeated blocks (in tape append)
- JJ = no.of blocks repeated (in tape append)
- KK = no. errors found in the data compare after the test write

11.6 EPCOV3: XU1120 STC ERROR RATE EVALUATION PROGRAM

PROGRAM PURPOSE

To evaluate the STC subsystem error rate under highly critical operating conditions.

HARDWARE REQUIRED

RAM board (min. 256 KB), STC controller boards (G0200/B G0201/B), Streaming Cartridge Tape unit (XU1120).

N.B.

The program can be run only on STC controllers with firmware releases no earlier than 7.0.

WARNING

This program includes tape write operations so the operator should first ensure that data on the tape can be destroyed.

OPERATING PROCEDURE

Refer to section 1.3.2.

11.6.1 TEST DESCRIPTION

Refer to section 11.5.1 of the SCTER7 program.

11.6.2 ERROR MESSAGES

Refer to section 11.5.2 of the SCTRE7 program.

11.7 CPCOV1: CIPHER ERROR RATE FOR PCOV PROGRAM

PROGRAM PURPOSE

To evaluate the STC subsystem error rate under critical operating conditions using read, write and append operations and also to test the service functions such as erase, pause, rewind and preconditioning.

HARDWARE REQUIRED

RAM board (min. 256 KB), STC controller boards (G0200/B and G0342) and Streaming Cartridge Tape unit (XU 1130).

N.B.

The program can be run only on STC controllers with firmware releases no earlier than 8.0.

WARNING

This program includes tape write operations so the operator should first ensure that data on the tape can be destroyed.

OPERATING PROCEDURE

Refer to section 1.3.2.

11.7.1 TEST DESCRIPTION

See the corresponding section (par. 11.5.1) of the SCTER7 program description.

11.7.2 ERROR MESSAGES

See the corresponding section (par. 11.5.2) of the SCTER7 program description.

11.8 STC5E2: ARCHIVE 5945C STC (45/60 MB) ERROR RATE PROGRAM

PROGRAM PURPOSE

To measure the error rate of the STC subsystem under critical operating conditions.

HARDWARE REQUIRED

ARCHIVE 5945C STC (45/60 MB) and tape, G0417 and G0418 controller boards.

OPERATING PROCEDURES

Refer to section 1.3.2.

11.8.1 DESCRIZIONE DEI TEST

For tests 1, 2, 3, 4 and 6 refer to same test described in section 11.5.1 of the SCTER7 program.

For tests 5 and 7 refer to test 5 described in section 11.5.1.

For test 8 refer to test 7 of the same section.

11.8.2 ERROR MESSAGES

In case of errors check/ change the controller board or the STC unit.

- **UNKNOW ERROR**
- **ERROR DURING INITIALIZATION PHASE**
- **INCHOERENT CONTROLLER ANSWER**
- **INCHOERENT CONTROLLER STATUS**
- **ILLEGAL COMMAND**
- **COMMAND ABORTED**
- **CDM QUEUE FULL**
- **SPEED ERROR DETECTED**
- **SW TIME OUT DETECTED DURING I/O**
- **READ RETRY LEVEL OVERFLOW**
- **TRACK OR BLOCK IDENTIFIER FIELD WRONG RECEIVED TRACK XX BLOCK YY**
- **EOD FLAG DURING WRITE OPERATION**

- **FM FLAG DURING WRITE OPERATION**

In case of the following messages check/change the tape.

- **ERROR DURING I/O: CARTRIDGE CRASH**

SUMMARY ERROR MESSAGES

At the end of the program the following summary messages are displayed:

```
     --- TAPE TRANSFER SUMMARY ---
         TRACK TT (ALL TRACKS)
=======================================
|READ BLOCKS:              |    AA     |
|OPERATION(S) WITH REPET.:|    BB     |
|REPEATED BLOCK(S)         |    CC     |
|ECC RECOVERED BLOCK(S):   |    DD     |
|FILE MARK(S):             |    EE     |
---------------------------------------
|WRITTEN BLOCKS:           |    FF     |
|OPERATION(S) WITH REPET.:|    GG     |
|REPEATED BLOCK(S):        |    HH     |
|FILE MARK(S):             |    II     |
---------------------------------------
|APPENDED BLOCKS:          |    JJ     |
|OPERATION(S) WITH REPET.:|    KK     |
|REPEATED BLOCK(S)         |    LL     |
|FILE MARK(S):             |    MM     |
---------------------------------------
|COMPARE ERROR(S)          |    NN     |
=======================================
```

Where:

- TT = track summary refers to

- ALL TRACKS = when summary is valid for all tracks

RESULTS OF READ OPERATIONS:

- AA = number of blocks read

- BB = number of operations with repeated blocks

- CC = number of blocks repeated

- DD = number of blocks recovered using ECC

- EE = number of "File Mark" read

RESULTS OF WRITE OPERATIONS:

- FF = number of blocks written

- GG = number of operations with repeated blocks
- HH = number of repeated blocks
- II = number of "File Mark" written

ADDED ON TAPE:

- JJ = number of blocks added
- KK = number of operations with repeated blocks
- LL = number of blocks repeated
- MM = number of "File Mark" written

RESULTS OF COMPARISON TESTS AFTER WRITING ON TAPE

- NN = number of errors found

11.9 STC5T3: G0417 AND G0418 TEST PROGRAM

PROGRAM PURPOSE

To test and diagnose the STC sub-system, comprising two printed circuit boards and a magnetic tape peripheral unit.

HARDWARE REQUIRED

ARCHIVE 5945C (45/60 MB) STC and tape, G0417 and G0418 controller boards,

WARNING

This program is valid only for firmware release 1.2 (and subsequent releases)

OPERATING PROCEDURE

Refer to section 1.3.2.

11.9.1 TEST DESCRIPTION

1) RESET AND SELFDIAGNOSTIC TEST

This test checks out the status of the controller after the autodiagnostic test and after a Software Reset.

2) CHECK COMMAND AND STATUS PORT TEST

The Command/Status Port is checked by writing data on the command port and then checking that the data written is read on the Status port.

3) READ/WRITE VECTOR INTERRUPTS TEST

A number of vectors are written on the command port and then issued.

4) NON MASKABLE INTER. GENERATION TEST

Checks the controller's ability to detect and indicate an error on the OLIBUS after a write operation has been initiated to an address reserved for the PROM.

5) READ DATA IN MAIN MEMORY TEST

This test checks the controller's ability to address and read system memory. A buffer is compiled in the system memory then the buffer is read and compared with the original pattern.

6) WRITE DATA IN MAIN MEMORY TEST

The controller's ability to address and write system memory is tested. Writes 16kB pattern in system memory then checks the data written.

7) LOAD/STORE IN MAIN MEMORY TEST

Checks the systems ability to exchanged data between System Memory and local memory. Compiles in local memory data read from the system memory then transfers part of this data to system memory and verifies the data transfered.

8) MEM/MEM DMA CONTROLLER TEST

Checks the systems ability to exchanged data from different areas in local memory. A program written in Z8002 language is transfered into RAM then the program loaded is executed. The system then checks if the program has been executed correctly.

9) PU TYPE TEST

Identifies the PU by reading the "identity" switch setting.

10) MOTOR SPEED AND POSITION HEAD TEST

Checks that the motor functions correctly by checking the motor speed and the positioning of the head.

11) WRITE DATA BLOCK OLIVETTI MODE TEST.

Transfers in local memory a program written in Z8002 code which instructs the controller to access a data block from system memory and write this (in Olivetti mode) on track 0 of the tape.

12) READ DATA BLOCK OLIVETTI MODE TEST.

Transfers in local memory a program written in Z8002 code which instructs the controller to read (in Olivetti mode) the data block previously loaded on track 0 and verify the data read.

13) ERASE & READ DATA BLOCK OLIVETTI MODE TEST.

Erases a block on the tape then reads a block (in Olivetti mode).

14) WRITE DATA BLOCK QIC24 MODE TEST.

Transfers in local memory a program written in Z8002 code which instructs the controller to access a data block from system memory and write this (in Qic24 mode) on track 0 of the tape.

15) READ DATA BLOCK QIC24 MODE TEST.

Transfers in local memory a program written in Z8002 code which instructs the controller to read (in Qic24 mode) the data block previously loaded on track 0 and verify the data read.

16) ERASE & READ DATA BLOCK QIC24 MODE TEST

The test is the same as test 13 except that data is read in "Qic24 mode".

17) WRITE & SEARCH FILE MARK TEST.

Writes and seaches a File Mark (in Quic24 mode).

18) ERASE TEST.

Erases the whole tape.

19) WRITE DATA BLOCK ON ALL TRACKS.

Writes (in "modo Qic24") on the tape on track 9 and verifies the data written.

20) READ DATA BLOCK ON ALL TRACKS.

Reads (in "modo Qic24") the tape on track 9 and verifies that the data read is the same data previously recorded.

21) REWIND TEST

The tape rewind command is sent out to the peripheral unit. Controller status and peripheral unit status are checked at the end of the command.

22) PRECONDITIONING TAPE TEST

The tape tension command is sent to the peripheral unit using the PRECONDITIONING I/O routine. Controller status and peripheral unit status are checked at the end of the command.

N.B.

At the end of tests 11 to 21 the controller status and peripheral unit status are checked at the end of the command.

11.9.2 ERROR AND SERVICE MESSAGGES

Refer to section 11.4.2 of the STC404 program.

12.1 MTUER7: MTC3/MTU (XU 1705) ERROR RATE PROGRAM

PROGRAM PURPOSE

To discover the error rate during read and write operations on a CIPHER MTU.

HARDWARE REQUIRED

G0278/B controller, XU1750 CIPHER MTU (40 MB) and tape.

WARNING

A test pattern is written on the tape, therefore a dump operation should be made if data is to be preserved as the original data is destroyed.

The tests are significant only if the following conditions are respected:

- the read tests (9 and 12) must be preceded by a write test (4),
- The search file mark tests (6 and 7) must be preceded by the write file mark test (5).

NOTE

The read test 3, can be run alone as this test is automatically preceded by a write cycle. After tests 3 and 8 it will be necessary to operate the "rewind" key before any other tests can be run.

LOADING PROCEDURES

Refer to section 1.3.2.

12.1.1 TEST DESCRIPTION

TEST 1 - REWIND

The tape is rewound and set at LOAD POINT.

TEST 2 - TEST WRITE (error-rate)

A test pattern is written on the tape starting from the LOAD POINT and continuing for a total of 1,000 Mbytes; this operation requires several write runs.

TEST 3 - TEST READ (error-rate)

A pattern is first written on the tape from the LOAD POINT and the tape then read from this point. Several read passes are made from the LOAD POINT for a total 1,000 Mbytes of tape.

TEST 4 - WRITE RECORDS

A test pattern is written on part of the tape (maximum 2000 records) or on the whole tape depending on the selection made during the preprogramming stage.

TEST 5 - WRITE FILEMARK

The WRITE FILEMARK command is issued and the results observed. A filemark is written on the tape in its current position.

TEST 6 - SPACE FORWARD FILEMARK

The SPACE FORWARD FILEMARK command is issued and the results observed. Filemarks written earlier are searched for in a forward direction.

TEST 7 - SPACE REVERSE FILEMARK

The SPACE REVERSE FILEMARK command is issued and the results observed. Filemarks written earlier are searched for in a reverse direction.

TEST 8 - UNLOAD

The tape UNLOAD COMMAND is issued and the results checked; the tape should then be released from its feed mechanism.

TEST 9 - READ RECORDS FORWARD

The area selected in Test 4 is read in the forward direction.

TEST 10 - ERASE ALL

The ERASE command is applied to the whole tape and the results observed.

TEST 11 - ERASE 4 INCHES

The ERASE command for a 4" section of tape (4 x 2.54cm) is issued; the results are observed.

TEST 12 - READ RECORDS REVERSE

The area selected in Test 4 is read in the reverse direction.

12.1.2 ERROR AND SERVICE MESSAGES

If any of the following error messages are displayed check/change, in order, the controller, the tape, the MTU.

- ** READ/WRITE ERROR NOT RECOVER. ***
- ** READ/WRITE ERROR RECOVERABLE ***
- ** FILE_MARK DETECTED ****
- ** WRITE FILE_MARK ERROR ***
- ** READ/WRITE PARITY ERROR ***
- ** READ/WRITE TIMING ERROR (HW)***
- ** READ/WRITE RUN_AWAY ERROR ***
- ** RECORD LENGTH RECORDING IS DIFFER.**
- ** P.U. BUSY - COMMAND REJECTED ***
- ** P.U. OFF_LINE -COMMAND REJECTED **
- ** P.U. REWINDING _ COMMAND REJECTED **
- ** P.U. ABSENT ***
- ** TAPE WRITE PROTECT ***
- ** TAPE LOAD_POINT ON REVERSE COMM. **
- ** END OF TAPE ON FORWARD COMMAND **
- ** COMMAND REJECTED FROM P.U.**
- ** HARDWARE ERROR ***
- ** SPEED NOT SELECTED AFTER SELECT_COMM**
- ** FAULTY HARDWARE DURING REWINDING **
- ** FAULTY HARDWARE DURING UNLOADING **
- ** P.U. ABSENT TO NOOPER COMMAND **
- ** HARDW. ERR. EOT POSITION **
- ** MAIN MEMORY ACCESS TIME_OUT **
- ** MEMORY ERROR ***
- ** CONTROLLER HW_ERROR **

- ** INTERRUPT NOT PROGRAMMABLE **
- ** NETWORK INTERRUPTION ERROR **
- ** GENERIC HARDWARE ERROR **
- ** DMA ERROR (not resettable)
- ** DMA ERROR ***
- ** CONTROLLER IS ALWAYS RESET_STATUS **
- ** ROUTINE I/O PARAMETERS ERROR ***
- ** HDW ERR. FLIP_FLOP (run away) **
- ** HDW ERR. FLIP_FLOP (timing error) **
- ** HDW ERR. FLIP_FLOP (parity err.)**
- ** HDW ERR. FLIP_FLOP (olibus timeout)
- ** HDW ERR. FLIP_FLOP (olibus p.err.)
- *** ERROR CODE OUT OF RANGE **
- *** CHECKSUM ERR. tx-rx ** (CHECKSUM error in comparison between pattern read on tape and the pattern selected and used in the write operations).
- *** TIME OUT ****

12.2 MTC304: CIPHER MTU G0278 (XU 1705) TEST PROGRAM

PROGRAM PURPOSE

To test the CIPHER MTU.

HARDWARE REQUIRED

G0278/B controller, XU1750 CIPHER MTU (40 MB) and tape.

NOTE

If the UNLOAD test no. 17 is run (it may be removed in the preprogram phase), the tape unit goes off line.

The tests are subdivided into two groups: tests 1 to 8, which concern only the controller and tests 9 to 17, which involve both controller and tape.

All the tests can be run a number of times, with the exception of test 17 (Unload). Before tests 12, 13 and 14 can be run, test 11 (in which a standard pattern is written) must be performed.

LOADING PROCEDURES

Refer to section 1.3.2.

12.2.1 TEST DESCRIPTION

The program is made up of 17 diagnostic tests designed to check that the control board and tape are functioning correctly.

TEST 1 - TOTAL AND PARTIAL RESET TEST

Enables the controller by clearing the Reset and then tests the total and partial resets by checking the contents of the CONTROLLER STATUS PORT.

TEST 2 - INPUT/OUTPUT PORTS TEST

The Input/Output ports are checked by first writing to the COMMAND PORT and then running a check of the STATUS PORT.

TEST 3 - CHANNELS 1/2 OF 8253 TEST

A read/write test of channels 1 and 2 of the timer 8253. The two channels are programmed and timer operation is checked.

TEST 4 - READ/WRITE VECTORS INTERRUPTS TEST

The PSA is programmed with three different vectors and the interrupt vectors loaded into the timer. The responses to the interrupts generated by the timer (programmed in advance) are checked.

TEST 5 - READ IN MEMORY WRITE ON TAPE DMA TEST

A WRITE RECORD on tape command is simulated and a DMA read attempt made.

TEST 6 - READ ON TAPE WRITE IN MEMORY DMA TEST

A READ RECORD on tape command is simulated and a DMA write attempted.

TEST 7 - READ/WRITE FORWARD MEMORY FIFO TEST

Correspondence between the internal bus and the Olibus is tested.
A record is read in MAIN MEMORY, written in the FIFO buffer and then FORWARD written into MAIN MEMORY.

TEST 8 - READ/WRITE REVERSE MEMORY FIFO TEST

A record is read in MAIN MEMORY, written in the FIFO buffer and then REVERSE written into MAIN MEMORY.

TEST 9 - TAPE SELECT AND SPEED TEST

The tape and tape speed select command is issued according to the parameters entered in the preprogramming phase and the results checked.

TEST 10 - TAPE DIAGNOSTIC PORT TEST

A number of commands are issued to the tape unit and the diagnostic port is then checked.

TEST 11 - WRITE FILE MARK/RECORDS/REWIND TEST

A write record with sample pattern (%AA55) command, FILE MARK command and REWIND command are issued; progress is checked.

TEST 12 - READ FORWARD/REVERSE RECORDS TEST

A record FORWARD read and a REVERSE read are performed and results checked.

TEST 13 - SEARCH FORWARD/REVERSE FILE MARK TEST

FILE MARK search FORWARD and REVERSE commands are issued and the results checked.

TEST 14 - SPACE FORWARD/REVERSE RECORD TEST

Record space FORWARD and REVERSE commands are issued and the results checked.

TEST 15 - WRITE EDIT READ REVERSE EDIT TEST

A record re-write with new data command is issued and the record read (WRITE EDIT e READ EDIT).

TEST 16 - ERASE VARIABLE LENGTH TEST

An erase command of approx 1 inch (2.54cm) of tape is issued and the results are checked.

TEST 17 - UNLOAD TEST

The tape UNLOAD command is issued and the results are checked. The operator is specifically asked in the preprogramming phase if this test is to be performed as the tape goes OFF LINE on completion of the test.

12.2.2 ERROR MESSAGES

The error messages listed below are sub-divided into groups, each group referring to a specific test.

If any errors are found during tests 1 to 8, check/change the MTU; If errors are found during tests 9 to 17 check/change, in order, the controller MTU, tape, the MTU (unless otherwise stated).

TOTAL AND PARTIAL RESET TEST

Ver. exit signal "STATN/TYPEN"
Ver. ENIRO/ SDMAO/ RWTAO/ INTRO signal stuck at "0"
Ver. RESFN signal stuck at "0/1"
Ver. in C05 type different from %62

INPUT/OUTPUT PORTS TEST

Ver. RWTAO/ DDMAO/ SDMAO/ ENIRO/ INTRO signal stuck at "0/1"

CHANNEL 1/2 OF 8253 TEST
Ver. WRCON RECON IND00=0/1,IND04=0/1
Ver. intern bus date or change timer
Ver. COBYN=0/1 or change timer
Ver. EVALO=0/1 WRCIN=0/1 COBYN=0/1
Ver. FEVLN=0/1 ILWDA=0/1 READN=0/1
Ver. intern counter change timer
Ver. IDBYN=1 TIMEO=0 or counter P08
Ver. IDBYO=0/1 T10C0 TIME1 TIMEO=1
Ver. RESFO=0/1 AZTIN=0/1 TIMEO=0 READO=0/1

READ/WRITE VECTORS INTERRUPTS TEST

Ver. vett. int. %XX on DKL7 in A05 (check the interrupt vector %XX..., where XX = 5A/C3/A4)
Ver. int. req. from TIMEO to OUVIA (check the interrupt request from etc.)
Ver. int. req. from CIFCO to OUVIA
Ver. int. req. from INTRO to OUVIA
Int. req. from TIME1 to TIMEO INTRO=0
Int. req. from IDBYO to CIFCO INTRO=0
Ver. ENIRO=0 LINTN=1 VINTN=1 VINTO=0 OUVIA=1
Int. req. from INTEO to INTRN INTRO=0

READ IN MEMORY WRITE ON TAPE DMA TEST

```
Ver. EVALO=1 RESFN not ok VUOTN=0
Ver. IGOOO=0/1 VUOTN=1 CWORN=0/1
Ver. signals CWORN or INDOO IND04
Ver. IDBYN=1/0 CUFIN=0/1 ILWDA=1
Ver. signal CWORN/COBYO or change timer
Ver. signals WRCIN, CWORN and ILWDA=0
Ver. FITR1=1 VUOTO=1  LREDO=1
Ver. IDBYN=1 CIFCO=0 INTRO=1
Ver. ATEWO=0 RWTAO=0 ATIEO=0 TIERO=0
Ver. PARIN=0 LEPT1=1 LRPON=0 ERPTO=0
Ver. signals REDYB=1 TIOBO=1
Ver. signals NOMI1=0 PAERO=0
```

READ ON TAPE WRITE IN MEMORY DMA TEST

```
Ver. IDBYN=0 READN=0/1
Ver. signals CWORN or INDOO IND04
READN=0/1 EVALO=0 or change timer
Ver. signals IDBYN=1 INTRO=1 VUOTN=0 ILWDA=0
Ver. signals WRCIN and CWORN
Ver. signal COBYO or change timer
Ver. ATEWO=0 RWTAO=0 ATIEO=0 TIERO=0
Ver. PARIN=0 LEPT1=1 LRPON=0 ERPTO=0
Ver. signals REDYB=1 TIOBO=1
Ver. signals NOMI1=0 PAERO=0
```

READ/WRITE FORWARD MEMORY FIFO TEST

```
Ver. IREVA=1 DDASN MALEN f.1.05
Ver. DINOO/70 DOUOO/70 f.1.05
Ver. 1BYTO ENW1N or MALEN DDASN
Ver. 2BYTO ENW2N or MALEN DDASN
Ver. ATEWO=0 RWTAO=0 ATIEO=0 TIERO=0
Ver. PARIN=1 LEPT1=0 LRPON=1 ERPTO=1
Ver. FITR1=1 VUOTO=0 LREDO=1
Ver. signals REDYB=1 TIOBO=1
Ver. signals NOMI1=0 PAERO=0
Ver. signal TIMEO=0 f.1.01 P08
Ver. RESFN 1/0 TIERO/ ERPTO/ TIMEO/ TIOBO/ PAERO/ LREDO not 0
```

READ/WRITE REVERSE MEMORY FIFO TEST

```
Ver. IREVA=0 DDASN MALEN f.1.05
Ver. DINOO/70 DOUOO/70 f.1.05
Ver. 1BYTO/2BYTO ENW1N/ENW2N or MALEN DDASN
Ver. ATEWO=0 RWTAO=0 ATIEO=0 TIERO=0
Ver. PARIN=1 LEPT1=0 LRPON=1 ERPTO=1
Ver. FITR1=1 VUOTO=0 LREDO=1
Ver. signals REDYB=1 TIOBO=1
Ver. signals NOMI1=0 PAERO=0
```

TAPE SELECT AND SPEED TEST

Err. signal IRDYN=0 tape not ready
Err. signal IEOTN=0 end of tape
Err. signal ILDPN=1 not load point
Err. signal IFBYN=0/1 formatter busy
Err. signal ISPEN=0/1 verify speed
Err. signal IFMKO=1 file mark
Err. signal ICERO=1 correctable error
Err. signal IHERO=1 uncorrectable error
Err. signal IRWDN=1 rewind
Err. signal IDBYN=1 data busy
Ver. signals IGOOO IDBYN INTRN=1
VERIFY SWITCHES ON BOARD PLEASE (check that switches 1 and 2 on the board are in the 0 position)

TAPE DIAGNOSTIC PORT TEST

Ver. signal IREWO/ IFEOO/ IREVA /IWFMA/ IEDIA/ IERAA/ IWRTA not 0/1
Ver. signal DIAG1 on F10/1-19

WRITE FILE MARK/RECORDS/REWIND TEST

TIERO=1 timing error = TIERO=1
ERPTO=1 parity error in read tape
TIMEO=1 time_out on data exchange
TIOBO=1 time_out on olibus during DMA
PAERO=1 parity error during DMA
LREDO=1 length record different
INOLO=1 Ver. signal tape off line
IHERO=1 UNCORRECTABLE ERROR FROM TAPE
ICERO=1 CORRECTABLE ERROR FROM TAPE
IFMKO=1 Ver. signal file mark
ILDPN=1 Ver. signal load point
IEOTN=0 Ver. signal end of tape
IFBYN=1 Ver. signal formatter busy
IRWDN=1 Ver. signal rewind
IFPTN=0 Ver. signal file protect
IRDYN=0 Ver. signal tape not ready

READ FORWARD/REVERSE RECORDS TEST

Messages for this test are the same as those for the WRITE FILE MARK/RECORDS/REWIND TEST

SEARCH FORWARD/REVERSE FILE MARK TEST

Messages for this test are the same as those for the WRITE FILE MARK/RECORDS/REWIND TEST

SPACE FORWARD/REVERSE RECORD TEST

Messages for this test are the same as those for the WRITE FILE MARK/RECORDS/REWIND TEST

WRITE EDIT READ REVERSE EDIT TEST

Messages for this test are the same as those for the WRITE FILE MARK/RECORDS/REWIND TEST

ERASE VARIABLE LENGTH TEST

Messages for this test are the same as those for the WRITE FILE MARK/RECORDS/REWIND TEST

UNLOAD TEST

- IRDYN=0 tape not ready before unload
- BADLY UNLOAD FASE
- Err. INOLO=0 not off line after unload

12.3 FJMTUS: MTU (XU 1705)/FUJITSU (XU 1700) DUMP/RESTORE PROGRAM

PROGRAM PURPOSE

This program tests the CIPHER MTU and FUJITSU HDU in dump/restore operations (i.e. a sample pattern chosen by the operator in the preprogram phase is transferred from tape to hard disk and vice versa and then comparison tests are made with the original data to see if there are any errors).

HARDWARE REQUIRED

G0278/B controller, XU1750 CIPHER MTU (40 MB) and tape, G0301/A and G0302/A controller boards, XU1700 HDU (FUJITSU M2312K, 60 MB).

WARNING

Initial contents of both tape and disk are destroyed in this test program.

Care should be taken in selecting the test sequence, as the pattern entered is used both in writing on one peripheral and checking on the other. The sequences proposed below are considered to be most significant and should be adhered to:

1-4-8,
2-5-7,
9-1-9-3-8,
9-2-5-9-6.

LOADING PROCEDURES

Refer to section 1.3.2.

12.3.1 TEST DESCRIPTION

TEST 1 - WRITE MTU

The sample pattern stipulated in the preprogram is written on the tape; the results of the operation are then analysed.

TEST 2 - WRITE FUJITSU

The hard disk is written on the section specified in the preprogram. Again, the sample pattern is used and the results are analyzed.

TEST 3 - RESTORE FORW (MTU => FUJI)

A "Restore Forward" operation (tape contents transferred forward from magnetic tape to hard disk) is performed; the results are analyzed.

TEST 4 - RESTORE REV (MTU => FUGI)

A "Restore Reverse" operation (tape contents reverse transferred from magnetic tape to hard disk) is performed; the results are analyzed.

TEST 5 – DUMP (FUJITSU => MTU)

A "Dump" operation (contents of hard disk transferred to the magnetic tape) in normal or streaming mode, depending on selection made in pre-program; the results are analyzed.

NOTE

The DUMP and RESTORE operations performed in tests 3, 4 and 5 are made with overlapping commands so that simultaneous operation of the two units can be checked.

TEST 6/7 – VERIFY MTU FORWARD/-VERIFY MTU REVERSE

The magnetic tape is checked in forward and reverse and contents stored compared with the sample pattern.

TEST 8 – VERIFY FUJITSU

The hard disk is checked by comparing the contents stored with the sample pattern.

TEST 9 – REWIND MTU

The REWIND command is issued and the results observed.

12.3.2 ERROR AND SERVICE MESSAGES

ERROR/SERVICE MESSAGES DUE TO HDU:

If any of the following error messages are displayed check/change, in order, the HDU controller and/or the HDU.

- MEMORY DATA COMPARE ERROR
- PERIPHERAL CONTROL SYSTEM BUSY -DISK-
- DRIVE IN PERMANENT FAILURE -DISK-
- DRIVE IN TRANSITORY FAILURE -DISK-
- PU FUJ. NOT READY -DISK-
- HARDWARE ERROR -DISK-
- TIME OUT ERROR -DISK-
- INTERRUPT NOT RECEIVED -DISK-
- SEEK INCOMPLETE -DISK-
- UNEXPECTED INTERRUPT RECEIVED -DISK-
- SYSTEM BUS ERROR -DISK-
- SOFTWARE ERROR -DISK-
- OPERATION NOT EXECUTABLE -DISK-
- PU IN WRITE PROTECT CONDITION -DISK-
- UNKNOWN PU -DISK-
- ABSENT PU -DISK-
- IDENTIFIER ERROR -DISK-
- SYNC MISSING -DISK-
- SECTOR NOT FOUND -DISK-
- WRONG TX_LENGTH -DISK-
- MEMORY TIME_OUT -DISK-
- MEMORY ERROR -DISK-
- DRIVE BUSY -DISK-
- DRIVE IN FAILURE -DISK-

- DRIVE ABSENT -DISK-
- ECC ERROR -DISK-
- DATA ERROR -DISK-
- ERROR DURING READING/WRITING PHASE -DISK-

ERROR/SERVICE MESSAGES DUE TO MTU:

If any of the following error messages are displayed check/change, in order, the MTU controller, tape and/or the MTU.

- READ/WRITE ERROR NOT RECOVER. -TAPE-
- READ/WRITE ERROR RECOVERABLE -TAPE-
- FILE_MARK DETECTED -TAPE-
- WRITE FILE_MARK ERROR -TAPE-
- R/W PARITY ERROR -TAPE-
- READ/WRITE TIMING ERROR (HW) -TAPE-
- READ/WRITE RUN_AWAY ERROR (a non-recorded section of tape, longer than the maximum allowed, has been found).
- RECORD LENGHT IS DIFFER.-TAPE-
- P.U. BUSY - COMMAND REJECTED -TAPE-
- P.U. OFF_LINE -COMMAND REJECTED -TAPE-
- P.U. REWINDING -COMMAND REJEC.-TAPE-
- P.U. ABSENT -TAPE-
- TAPE WRITE PROTECT -TAPE-
- LOAD_POINT ON REVERSE COMM.-TAPE-
- END OF TAPE DETECTED -TAPE-
- COMMAND REJECTED FROM P.U.-TAPE-
- P.U. NOT READY YET -TAPE-
- SPEED NOT SELECTED AFTER SELECT -TAPE-
- FAULTY HDW DURING REWINDING -TAPE-
- HARDW. ERR. EOT POSITION -TAPE-
- MAIN MEMORY ACCESS TIME_OUT -TAPE-
  in MAIN MEMORY

- MEMORY ERROR -TAPE-
- CONTROLLER HW ERROR -TAPE-
- INTERRUPT NOT PROGRAMMABLE -TAPE-
- NETWORK INTERRUPTION ERROR -TAPE-
- GENERIC HARDWARE ERROR -TAPE-
- DMA ERROR (NOT RESETTABLE)-TAPE-
- DMA ERROR -TAPE-
- MTC3 IS ALWAYS RESET-STATUS -TAPE-
- ROUTIN I/O PARAMETERS ERROR -TAPE-
- HDW ERR. FLIP FLOP (RUN AWAY) -TAPE-
- HDW ERR. FLIP FLOP (TIMING ERROR) -TAPE-
- HDW ERR. FLIP FLOP (PARITY ERR.) -TAPE-
- HDW ERR. FLIP FLOP (OLIBUS TIMEOUT) -TAPE-
- HDW ERR. FLIP FLOP (OLIBUS P.ERR.) -TAPE-
- ERROR CODE OUT OF RANGE -TAPE-
- CHECKSUM ERR. TX-RX -TAPE- (checksum error found in the comparison of the pattern read on the tape and the one selected for use in the write operations)
- TIME OUT -TAPE- = TIME OUT

12.4 120FC3: MTU (XU 1705)/FUJITSU (XU 1703) DUMP/RESTORE PROGRAM

PROGRAM PURPOSE

This program tests the CIPHER MTU and FUJITSU HDU in dump/restore operations (i.e a sample pattern chosen by the operator in the preprogram phase is transferred from tape to hard disk and vice versa and then comparison tests are made with the original data to see if there are any errors).

HARDWARE REQUIRED

G0278/B controller, XU1750 CIPHER MTU (40 MB) and tape, G0301/A and G0302/A controller boards, XU1700 HDU (FUJITSU M2312K, 60 MB).

WARNING

Initial contents of both tape and disk are destroyed in this test program.

Care should be taken in selecting the test sequence, as the pattern entered is used both in writing on one peripheral and checking on the other. The sequences proposed below are considered to be most significant and should be adhered to:

1-4-8,
2-5-7,
9-1-9-3-8,
9-2-5-9-6.

LOADING PROCEDURES

Refer to section 1.3.2.

12.4.1 TEST DESCRIPTION

This test is the same as described in section 12.3.1. of the FJMTU5 program.

12.4.2 ERROR MESSAGES

Refer to section 12.3.2. for list of error messages.

13.1 TS5016: XU5010 (VIA INTEGRATED CONTROLLER) TEST PROGRAM

PROGRAM PURPOSE

To test the subsystem hardware consisting of the HDU and controller using the test tracks only.

HARDWARE REQUIRED

INTEGRATED HDU controller, HDU.

PRELIMINARY WARNING

The disk used must be correctly formatted. Any faults in the user section will impair correct program execution.

NOTE

The HDU need not be connected in the first four tests.

LOADING PROCEDURE

Refer to section 1.3.2.

13.1.1 TEST DESCRIPTION

Interrupts are disabled for all tests (except the INTERRUPT test). Certain tests are made on one disk sector only. The section used is treated as the first physical sector by the integrator controller (i.e. the second sector after the INDEX signal). This method facilitates oscilla-scope (or other instrument) readings.

TEST 1 - SLOT TEST

The slot number entered in the pre-program is checked to see if it contains the correct controller.

TEST 2 - DISABLE INTERRUPT TEST

An interrupt signal is generated via an appropriate routine. A check is made to ensure that the signal is set and that no interrupt signals have been generated by the CPU. The controller interrupt is then reset and a check made to see that the corresponding signal has been reset. The cycle is repeated until all the interrupts in the PSA are tested.

TEST 3 - INTERRUPT TEST

An interrupt signal is generated via an appropriate routine. A check is made to verify that this signal is set and that an interrupt is generated on the correct vector in the CPU.

TEST 4 - DMA TEST

The segment adjacent the segment containing the program code is treated as a sample segment and tested as follows:

- A test pattern is written in the first half of the segment.
- The second half of the segment is set to zero.
- The first half is then transferred into the second half of the segment using the HDU internal buffer.
- The two halves of the segment are then compared to see if they are the same.
- The above operations are repeated with the test pattern written on the second half of the segment and direction of transfers reversed.

The other segments are tested as follows:

- The test pattern is rewritten in the sample segment.
- The contents of the sample segment are transferred into a segment to be tested via the HDU internal buffer.
- The contents of the sample segment are then compared with the contents of the segment under test and checked to see if they are the same.
- The above operations are repeated until an unmapped segment is found or 10 segments are tested or when the test on segment 50 is completed.

TEST 5 - COMMAND CHANNEL TEST

A character string is transferred from the controller to the disk unit. The character string is then re-transferred from the disk unit to the controller. The cycle is repeated 256 times.

TEST 6 - PU EXTENDED DIAGNOSTIC TEST

The extended diagnostic command is sent out and checked.

TEST 7 - PU CODE TEST

A check is made to see that the correct disk unit has been selected in the pre-program and checks that the disk has the right number of recording surfaces.

TEST 8 - PU TYPE TEST

A check is made to ensure that the correct disk type is used and the firmware update level is displayed.

TEST 9 - SEEK TEST

The head setting and selection system are tested as follows:

- The first sector on track is read.
- A check is made to find out if the identifier read is correct; if not, subsequent sectors are read until a correct identifier is found.
- The cylinder identifier is checked to insure that it corresponds to the cylinder on which the setting was made.
- The test is repeated on other heads until a number of cylinders have been tested.

TEST 10 - READ TEST

The systems ability to read a sector is checked by reading the diagnostic track and verifying if the data read is correct.

TEST 11 - MULTISECTORS READ TEST

The system is checked to ensure it can perform correct multisector readings by repeating the READ test on two other sectors.

TEST 12 - WRITE PHYSICAL TEST

A test pattern is recorded on the first sector of the track under test. The sector is then read and checked. The sector is again tested but with a different test pattern.

The test is repeated on other sectors until all recording surfaces are read.

TEST 13 - MULTISECTORS WRITE PHYSICAL TEST

A number of recordings are made, the length varying from 2 to 5 sectors, after each recording the data is read and compared with the data written. This procedure is repeated until all recording surfaces are tested.

TEST 14 - VERIFY PHYSICAL TEST

Three adjacent sectors are recorded and read to check that the data has been written correctly. A pattern differing by 1 bit from the previous pattern is then recorded on a sector. A check is then made to see if the change is detected. This procedure is repeated with the test bit in a different position until all bits of the three sectors are tested.

TEST 15 - WRONG IDENTIFIER TEST (identifier)

To ensure operation only on the required sector, the entire track is erased. A pattern with a correct identifer layout is recorded on the first physical sector, which is then read to confirm that the identifier is correct. The sector is recorded again with the same identifier as before but this time with 1 bit less (CRC incorrect). On re-reading the sector, the controller should detect the error. The latter part of the test is repeated until all the identifier bits (except for the CRC field) are tested.

TEST 16 - WRONG IDENTIFER TEST (CRC)

This test is carried out in the same way as Test 15, but the sector is re-recorded with the same CRC field except for one bit. The final steps are repeated until all the bits of the CRC field have been tested.

TEST 17 - RECOGNISED IDENTIFER TEST

Again, this test is carried out in the same way as Test 15, the sector is re-recorded with same identifier field except for one bit.

TEST 18 - ECC TEST (data field)

The entire track formatting is erased to ensure operation only on the required sector. A pattern with a correct data field format is recorded on the first physical sector; the sector is then read and checked before being recorded again, this time with an error in the data field. When the sector is read again, the error should be signalled by the controller, and, where the error burst generated is less than 11 bits, the data in memory should be correct. The latter steps are repeated, simulating error bursts of up to 33 bits and in three diffferent positons within the data field.

TEST 19 - ECC TEST (ECC field)

This test is carried out in the same way as Test 18, but, when the sector is re-recorded it is with an error in the ECC field. The latter steps are repeated, simulating error bursts of up to 22 bits.

TEST 20- DATA SYNC TEST

- The entire track formatting is erased to ensure operation only on the required sector.

- A pattern of a sector in which the second byte of the data field has the hexadecimal character 55 is recorded on the first physical sector.

- The sector is then read to check that locking occurred on the first synchronization character.

- The pattern is recorded again; this time without the synchronization character.

- The sector is then reread and the data mark not found should be signalled.

- The last two procedures are repeated placing the hexadecimal character 55 in position so that the controller again finds the read signal active when the SECTOR PULSE signal of the next sector is found.

- The pattern is again recorded; this time with the synchronization byte different from the standard by one bit and with hex. 55 still in the second byte of the data field.

- The sector is read again - locking should occur on the second byte of the data field. The latter steps are repeated until all the bits of the synchronization character are tested.

TEST 21 - WRITE TEST

This test is used to verify writing occurs correctly on specified sectors with the margin set:

- The test track is formatted and all sectors recorded except for the first sector.

- A known pattern is recorded on the first sector.

- The sector is then read using all margin combinations.

- The rest of the track should remain unaltered. Only one incorrect reading is needed for an error to be signalled. This procedure is repeated on all recording surfaces.

TEST 22 - MULTISECTORS WRITE TEST

The test track is formatted and a test pattern recorded on the first 2 sectors. The sectors are read using all margin combinations. Only one incorrect reading is needed for an error to be signalled. The procedure is repeated on all recording surfaces. Any faulty sector is skipped during track formatting.

TEST 23 - VERIFY TEST

- The contents of the test track are destroyed to ensure operation only on the first sector. A pattern of a sector with correct indentifier and data field is recorded on the first sector.

- A "verify" is run on the sector just recorded - no error should be signalled. The sector is recorded again, but this time an error is simulated.

- The "verify" is run again - the error should now be signalled. The last 2 steps are repeated 3 times, simulating comparison error, ECC error and ECC + comparison error.

TEST 24 - MULTISECTORS VERIFY TEST

- Test cylinder track 0 is formatted. The first 5 sectors are recorded, read and checked.

- The "verify" commands are run, simulating in memory errors in the recorded sectors.

13.1.2 ERROR MESSAGES

If an error occurs try changing the controller before the HDU.

- AFTER ECC CORRECTION
- SOME READ OPERATION SUCCESSFULLY
- ALL SECTORS ARE UNREADABLE
- ALL PHYSICAL READ ANSWERS ARE MARK ERROR
- EXTENDED DIAGNOSTIC ERROR
- CONTROLLER STATUS FLAGS BEFORE LAST I/O ROUTINE:
- BURST ERROR= ##
- P.U. ERROR ON 1 BYTE COMMAND
- P.U. HAS RETURNED A WRONG CODE
- COMPARE ERROR ON CHARACTER EXCHANGE
- OBS= XX EXP= YY
- DATA COMPARE ERROR
- THE I/O ROUTINE HAS RETURNED A CORRECT ANSWER BUT THE DATA IN MEMORY ARE WRONG
- CYL XXX HEAD YY

- ECC ERROR IN DATA FIELD HAS BEEN DETECTED AS ERROR IN ECC FIELD
- IDENTIFIER CYLINDER FIELD IS NOT EQUAL ON ALL HEADS
- MAYBE THE HEADS ARE NOT ALIGNED
- DMA ERROR WHILE READING FROM ADDRESS
- <<##>>####(######) OR WHILE WRITING TO
- ADDRESS <<##>>####(######)
- DMA DOES NOT START DURING READ OPERATION
- ECC ERROR IN ECC FIELD HAS BEEN DETECTED AS ERROR IN DATA FIELD
- ECC ERROR ON DATA FIELD
- ECC ERROR DETECTED BUT DATA FIELD IS GOOD
- VERIFY ERROR
- DATA MARK(SYNC) NOT FOUND
- MEMORY ERROR
- IDENTIFIER ERROR
- P.U. NOT ABLE TO WRITE
- TIMEOUT ERROR
- SECTOR NOT FOUND
- SUBSYSTEM ERROR
- TIME-OUT ON MEMORY ACCESS
- GENERATED ERROR FEATURE: WRONG DATA FIELD AND GOOD ECC
- GENERATED ERROR FEATURE: GOOD DATA FIELD AND WRONG ECC
- GENERATED ERROR FEATURE: WRONG DATA FIELD AND WRONG ECC
- EXPECTED ANSWER: R7=0004
- EXPECTED ANSWER: R7=0001
- P.U. FAULT
- THE FIRST BIT WRONG IS IN BYTE YYY BIT X OF DATA FIELD
- P.U. OR XD2829(FORMATTER) ARE NOT ABLE TO READ
- TEST FROM SEG. <<##>> TO SEG. <<##>>

- P.U. PERMANENT NOT READY
- GENERATED ERROR FEATURES: ALL SECTORS ARE GOOD WRITTEN
- HEAD SELECTION ERROR
- INVALID HEAD NUMBER
- RECOGNIZED ID. ######################
- REQUESTED ID. ######################
- ID. EXP ## #### ## ## OBS ## #### ## ##
- AN IDENTIFIER WITH WRONG CRC HAS BEEN RECOGNIZED AS GOOD
- INCOHERENT ANSWER IN R7 - POSSIBLE U.C. ERROR
- INCOHERENT ANSWER IN RECORD
- INCOHERENT ID. PATTERN
- INCOHERENT ECC ERROR
- INCOHERENT VERIFY ERROR
- INTERRUPT VECTOR LOADED: ###
- INTERRUPT VECTOR OBSERVED: ###
- UNEXPECTED INTERRUPT DETECTED: INTERRUPT VECTOR IS PROPERLY GENERATED
- INTERRUPT HARDWARE FAILURE
- INTERRUPT NOT DETECTED IN U.C.
- UNEXPECTED INTERRUPT PENDING CONDITION
- INTERRUPT DETECTED BUT THE INTERRUPT VECTOR IS WRONG
- INTERRUPT DETECTED BUT THE INTERRUPT VECTOR IS WRONG AND NOT EVEN
- UNEXPECTED INTERRUPT DETECTED: THE INTERRUPT VECTOR IS WRONG
- UNEXPECTED INTERRUPT DETECTED: THE INTERRUPT VECTOR IS WRONG AND NOT EVEN
- UP FW LEVEL= XXXX
- MARGINAL READ ON STANDARD DIAGNOSTIC TRACK FAILURE
- OFFSET : ####
- TIMEOUT ON FIRST COMMAND TO XU5010

- FAILURE IN COMMUNICATION PROTOCOL BETWEEN XD2829 AND XU5010
- THE WRONG SECTOR IS NOT DETECTED AS DEFECTIVE
- NOT DISCRIMINABLE ERROR
- ECC ERROR NOT DETECTED
- INTERRUPT LINE IN THE CONTROLLER IS NOT SET
- INTERRUPT LINE IN THE CONTROLLER IS NOT RESET
- NOT-DREAD DATA ARE NOT IN MEMORY
- FAILURE IN WRITING THE INTERNAL BUFFER
- P.U. NOT ANSWERING AT SELECTION
- P.U. NOT AVAILABLE
- P.U. BUSY
- THE WRONG SECTOR IS ##
- RECOVERABLE ECC ERROR HAS BEEN DETECTED AS UNRECOVERABLE
- SEEK ERROR)
- WRITE PHYSICAL DID NOT AFFECT THE SECTOR CONTENTS
- CONTROLLER STATUS FLAGS:
- DALEN=# STADN=# PED10=# PEOC0=#
  FUL12=# DMOK1=# GER10=# ZZZZZ=#
  FILU1=# FIZ01=# INZ01=# PRINT=#
  RISEN=# PAERO=# ERBU1=# ZZZZZ=#
  ERP01=# ERDA1=# ERCE1=# ERMA1=#
  ERTI1=# STAR1=# ERREO=# AEBE0=#
- CHARACTER '##' RECOGNIZED AS SYNC CHARACTER('55')
- THE FORMATTER DOES NOT DETECT THE ABSENCE OF SYNC CHARACTER
- TEST CANNOT RUN
- TEST IN SEG. <<##>>
- FB CYL HD ST CRC
- DATA TRANSFER ERROR BETWEEN FORMATTER AND INTERNAL CONTROLLER BUFFER
- TRACK SKIPPED
- NO READ OPERATIONS SUCCESSFULLY

- P.U. HAS RETURNED A WRONG TYPE
- SYNC CHARACTER FOUND NOT DISCRIMINABLE
- UNRECOVERABLE ECC ERROR HAS BEEN DETECTED AS RECOVERABLE
- P.U. NOT ABLE TO READ
- XU5010 FAILURE
- WRITE OPERATION AFFECTS MORE SECTORS THAN THE ONES REQUESTED
- THE CORRECTION PATTERN DOES NOT MATCH THE ERROR BURST
- IT HAS BEEN RECOGNIZED AN IDENTIFIER DIFFERENT FROM ONE EXPECTED
- WRONG SYNC CHARACTER HAS BEEN RECOGNIZED
- XD2829(CONTROLLER) OR XU5010 FAILURE
- XD2829 FAILURE
- XD2829(CONTROLLER) FAILURE
- XD2829(FORMATTER) FAILURE

13.2 S24151: XU5010 (VIA INT. CONTROLLER) INITIALIZATION PROGRAM

PROGRAM PURPOSE

To initialize cylinder 0.

HARDWARE REQUIRED

HDU controller board, XU5010.

PRELIMINARY WARNING

This program destroys user data. A dump operation should be made if data is to be saved.

LOADING PROCEDURE

Refer to section 1.3.2.

13.2.1 PROGRAM DESCRIPTION

The program initially checks for congruency between the logic name selected and the logic name of the HDU integrated controller and then initializes track 0, cylinder 0 sectors 7-8-9-10-11-12.

13.2.2 ERROR MESSAGES

If the congruency test for the logic name fails the following message is displayed and control returns to Monitor:

THE PRESENT CONTROLLER IN SLOT "XX" ANSWER PHYSICAL NAME "YY" INSTEAD OF "E4"

13.3 DIS011: XU5010 REGISTRATION (VIA INT. CONTROLLER) PROGRAM

PROGRAM PURPOSE

To register the XU5010 unit, to initialize cylinder 0, to initialize all the user sectors with the %0000 pattern and to initialize the test cylinders.

HARDWARE REQUIRED

HDU controller boards and XU5010.

WARNING

If a unit contains data which must not be lost, a disk DUMP should be made.

LOADING PROCEDURE

Refer to section 1.3.2.

13.3.1 PROGRAM DESCRIPTION

The program initializes cylinder 0 and all user sections with the pattern %0000.

If formatting is not required, only cylinder 0 is initialized.

If the disk is to be formatted, the ERMAP is NOT altered.

13.4 ER5013: XU5010 (VIA INT. CONTROLLER) ERROR RATE PROGRAM

PROGRAM PURPOSE

To evaluate the error rate of the XU5010 subsystem under critical conditions.

HARDWARE REQUIRED

HDU controller boards, XU5010.

PRECAUTIONARY NOTE:

As disk write operations are part of this program, the operator should ensure that data stored on disk can be destroyed.

LOADING PROCEDURE

Refer to section 1.3.2.

13.4.1 PROGRAM DESCRIPTION

The default sequence can be altered; however, note the following points:

1. Default sequence causes critical conditions which are significant.
2. If the program is being run on a HDU for the first time, to be significant, the first test must be a write test.

There are nine default patterns, which are particulary critical for this unit.

A normal program run entails the following steps:

- a congruency test to ensure that the HDU controller is in the correct slot
- HDU initialization
- Execution of the required tests
- Return of control to MONITOR

TEST 1 - WRITE FORWARD

Records a test pattern (comprising 9 patterns, one for each sector) on all tracks starting from track 0, head 0 through to last track, head 4. Under optimum conditons, the entire data surface is recorded without error, as the alternative tracks do not undergo checking.

TEST 2 - WRITE BACK

Records a test pattern (comprising 9 patterns, one for each sector) on all tracks starting from last track, head 0 through to track 0, head 4.

TEST 3 - READ FORWARD (TEST MODE)

Reads all tracks from track 0, head 0 through to the last track, head 4 and if selected by the operator makes a byte by byte comparison test with data read and original test pattern.

TEST 4 - READ BACK (TEST MODE)

Reads all tracks from last track, head 0 through to the track 0, head 4 and if selected by the operator makes a byte by byte comparison test with data read and original test pattern.

TEST 5 - READ RANDOM

Makes 2000 readings in random order, using an algorithm which generates pseudo-random numbers.

TEST 6 - READ FORWARD (MARGINATED MODE)

Reads as in READ FORWARD but in marginated mode. In addition access to alternative tracks is enabled in 4 separate runs with the following modes: strobe early/late track offset minus/plus.

TEST 7 - READ BACK (MARGINATED MODE)

To read the medium in marginated mode.

Reads as in READ BACKWARDS but in marginated mode and with the additional modes as decribed in READ FORWARD (MARGINATED MODE).

13.4.2 ERROR MESSAGES

Positioning error during a read operation:

A message indicating the cylinder, head and sector on which the error has been found. The program will then perform a HOME operation and re-issue the read command for the sector following the sector containing the error. Comparison tests, if requested, will be performed in memory after each error.

Data field errors

A message is displayed indicating the cylinder, head and sector associated with the error. The data on that sector is then tested to see if the error is in the data field or the ECC field. Comparison tests, if requested, will be performed in memory after each error.

Comparison errors

A message is displayed indicating the cylinder, head and sector associated with the error. Also displayed is the position of the first incorrect byte, the next 16 bytes together with the correct byte value.

13.5 VC5012: XU5010 (V1A INT. CONTROLLER) CORRECTION PROGRAM

PROGRAM PURPOSE

To check disk for defective tracks, assign alternative sectors/tracks and display or print contents of sectors.

HARDWARE REQUIRED

HDU controller boards, XU5010.

WARNING

The write operations in this program destroys user data. A dump operation should be made if data is to be saved.

LOADING PROCEDURE

Refer to section 1.3.2.

13.5.1 PROGRAM DESCRIPTION

TRACK VERIFY

A number of read cycles specified by the user (at least 1000) is made in order to verify a track.

SECTOR VERIFY

A number of read cycles specifed by the user (at least 1000) is made in order to verify a sector.

TRACK WRITE & VERIFY

Test patterns are recorded on a track followed by a read operation. The data read is then compared with the data written.

SECTOR WRITE & VERIFY

Test patterns are recorded on a sector followed by a read operation. The data read is then compared with the data written.

DISK DUMP

The contents of one or more sectors (up to 32) are printed or displayed in hexadecimal characters with their ASCII equivalents shown adjacent. Characters which cannot be printed are indicated with ".".

TRACK PROCESSING

The identifiers of a track are read and the track status displayed (01 = good; 0D = alternative; 0E = defective). Subsequently, track formatting can be made with the required modifications (selecting alternative cylinders/sectors etc.).

13.5.2 ERROR MESSAGES

Recoverable errors

```
CYL = XX  HEAD = XX  SECT = XX
Marginal mode: STR+ OF- (only for a marginate command)
ECC ERROR
RECOVERED
LENGTH BURST ERROR = XX
```

The message is displayed whilst a track or sector is being checked when the system encounters an error which is recoverable. Also displayed are details of the address where the error was found (cylinder, surface, sector), the margin used, the type of error and the burst length.

Non-recoverable errors

```
CYL = XX  HEAD = XX  SECT = XX
Marginal mode: STR+ OF- (only for a marginate command)
ECC ERROR
NOT RECOVERED
```

The message is displayed when the error is not recoverable. Also displayed are the address where the error was found (cylinder, surface, sector) and type of error.

Setting errors

```
FB = XX  CYL = XX  HEAD = XX  SECT = XX
ERROR ON IDENTIFIER
FB   EXPECTED XX  DETECTED YY
CYL  EXPECTED XX  DETECTED YY
HEAD EXPECTED XX  DETECTED YY
SECT EXPECTED XX  DETECTED YY
```

The message is displayed when the system is unable to access a specified address and gives details of the command, the error address (flag byte, cylinder, surface and sector), the type of error and the I/O routine response (in register R7) with the values expected and those received.

The faults listed below may occur in the Track Processing test:

```
FLAG BYTE NOT IDENTIFIED
ALL SECTORS O.K. - ALTERNATIVE SECTOR NOT EXISTING
DEFECTIVE ALTERNATIVE SECTOR
SECTOR XX DEFECTIVE - ALTERNATIVE SECTOR FREE
MORE THAN ONE WRONG IDENTIFIER
```

13.6 501TM1: XU5010 INTEGRATED ROTATION TIME MEASUREMENT TEST

PROGRAM PURPOSE

To calculate the rotation and positioning time of the HD unit.

HARDWARE REQUIRED

XU5010 hard disk unit and XU5010 sub-system.

OPERATING PROCEDURE

Refer to section 1.3.2.

13.6.1 TEST DESCRIPTION

TEST 1

This test calculates the HDU rotation time by initiating a read on a non existing sector which causes an interrupt to be generated and the system timer to be triggered. Then a further five reads are made and, on the last interrupt, the timer is stopped. The time measured between the first and last interrupt is the time taken for 10 revolutions of the HDU and is used to calculate the rotation time to an accuracy of 0.1%. When the time measured is greater than 1% of the average rotation time, an error message is displayed.

TEST 2

This test checks the positioning time of the HDU by using the system timer to determine the time taken to move track to track (9.999ms max), 144 tracks (43.999ms max) and 429 tracks (103.999ms max) in both the forward and reverse direction.

An error message is displayed at the end of the test if the maximum time is exceeded.

TEST 3

This test checks the positioning time of the HDU by using the system timer to measure the time taken to make successive seeks in steps defined by the operator from a lower cylinder to a higher cylinder and to return to the original cylinder. The test can be carried out on the whole disk or only on a section of the disk defined by the operator.

TEST 4

This test determines the positioning time of the XU5010 peripheral unit.

The operator enters the value of the lower cylinder and the higher cylinder used by the program to calculate and display the positioning time (SEEK) and return time.

If the lower cylinder is 0, the SEEK return is a "HOME" operation. Should the lower and higher cylinder be the same, the SEEK (or HOME) operation is not made and the message "TIME TOO SMALL TO BE MEASURED" is displayed.

13.6.2 ERROR AND SERVICE MESSAGES

If an error occurs try changing the controller first then the HDU.

- HARDWARE FAULT
- PERMANENT FAULT
- TEMPORARY FAULT
- ERROR ON IDENTIFIER
- ERROR ON READ COMMAND
- TIME OUT ON READ COMMAND
- DATA MARK NOT FOUND
- SECTOR NOT FOUND
- ERROR ON VERIFY
- U. P NOT AVAILABLE
- U. P. BUSY
- TIME OUT ERROR MEMORY ACCESS
- MEMORY ERROR
- SYITEM BUS ERROR
- INCOHERENT ANSWER
- U. P. NOT RECOGNISED

14.1 SASIT5: SASI3 AND P.U. TEST PROGRAM

PROGRAM PURPOSE

To check the operation of an XU5006 HDU when connected to a SASI interface.

REQUIRED HARDWARE

XU5006 HDU with DTC510 BP/BO controller, G0298 and G0299 controller boards,

PRELIMINARY WARNING

A dump operation should be made if data on disk is to be preserved.

LOADING PROCEDURES

Refer to section 1.3.2.

14.1.1 TEST DESCRIPTION

GENERAL

Tests 1 to 24 are carried out in numerical order. Any errors are treated as detailed below:

- ERRORS DURING TEST 1

  The test is repeated if more than one test is specified in the default program. If the fault does not clear the remaining tests are skipped.

- ERRORS DURING TEST 2 TO 14

  The program is looped so that the remaining tests (up to test 14) are carried out. All tests are repeated if more than one test is specified in the default program.

- ERRORS DURING TESTS 15 TO 24

  The test is repeated if more than one test is specified in the default program. The remaining tests are not executed unless the fault is cleared.

TEST 1 - ADAPTER CONTROLLER RESET TEST

This procedure resets the host adapter and controller and test that the system is correctly reset.

TEST 2 - SLOW HANDSHAKE TEST

This procedure checks the handshake protocol between the adapter and the controller with an internal loop back using the control and status port of the adapter.

TEST 3 - FAST HANDSHAKE TEST

This procedure permits the execution of the fast handshake protocol in which the signal SASEO is used to force a reply to a request (other than a read or write request). The SASEO signal is generated by a test circuit which accesses the SASI bus.

TEST 4 - VERIFY COMPARATOR TEST

This procedure checks the comparator logic. After checking the error line status, data is written on the SASI data out port. After processing, a comparison is made between the data on the INBUX and the data on the OUTBX.

TEST 5 - INTERNAL LOOP-BACK TEST

This procedure first makes a comparison check with the INBUX and OUTBX and two SASI transceivers, as already explained, and then checks the bus which enables the DMA logic by writing and reading in memory and checking that the data is unchanged.

TEST 6 - TIMER TEST

This procedure checks the three timer channels in their three normal function modes.

TEST 7 - DMA LOOP-BACK TEST

This procedure checks the DMA logic in loopback mode. Data is written in a memory location. The DMA is then enabled in write mode. The DMA lines are then inverted, two requests are generated and a check made to verify that the memory address is incremented and that it contains the same data as in the previous location.

TEST 8 - OVER MEMORY DMA TEST

This procedure attempts to address in DMA an address which is outside the memory boundary. The program verifies that the error pending and time-out signals are generated at DMA logic level of the host adapter.

TEST 9 - HISTORY PORT TEST

This procedure writes data in the history port and reads the same data in the command port until all values from %00 and %7F are covered or an error detected.

TEST 10 - DISCONNECT ADAPTER TEST

This procedure logically disconnects the adapter from the system by writing, when required, the controller port type incorrectly. This operation generates an NMI for I/O transfer error and substitutes a special routine in place of the standard routine.

TEST 11 - SPECIAL INTERRUPT TEST

This procedure generates a dummy interrupt by activating and then resetting a special interrupt line. If the system is not busy the flag to exit test is initially set and a test made to see if the interrupt pending bit is set in the adapter status port. After reset a test is made to ensure that the interrupt pending bit is no longer set and the exit test flag reset.

TEST 12 - SYSTEM INTERRUPT TEST

This procedure generates an interrupt to test the IRQ service interrupt logic. A vectored interrupt is loaded in a special HWD register. The system is then freed to generate a pending interrupt and a wait flag is set. If the system is not busy the exit test flag is set and the program goes into an IRQ wait loop, waiting for the special interrupt or the end of the wait period. A test is made to ensure that the special interrupt was received and then the interrupt line is reset.

TEST 13 - SWITCHES TEST

This test checks that the switches on the adapter board are set to a value other than %FF.

TEST 14 - COMMUNICATION ADP-CNT TEST

This test transmits an initialization command (contriniz) to the controller and waits for the acknowledgment from the controller. On receipt of acknowledgement the wait period is terminated (with contrinizend) and test finished.

TEST 15 - CONTROLLER AND P.U. TYPE TEST

This test checks the system configuration and displays the code identifier for the number of P.U. present. The program then resets the adapter and the controller and forces the P.U. under test to the "home" position.

TEST 16 - TRACKS IDENTIFIER TEST

This test carries out a number of seek and track checks, in forward and reverse mode, with different displacements and on different cylinders.

TEST 17 - TRACK IDENTIFIERS TEST

This test accesses in sequence two tracks per cylinder and tests the identifiers.

TEST 18 - READ DATA TEST

This test reads test patterns from five different sectors on each track of the diagnostic cylinder. These test patterns have been previously recorded for diagnostic purposes during the certification program.

TEST 19 - ECC NETWORK TEST

This test initially reads the addresses of the diagnostic write tracks from the read cylinder, forces a series of ECC errors which can be corrected by writing a string of data (%0 to %F) and then shifts this data through the sector forcing errors which cannot be corrected. The system then checks to see that the error has been correctly signalled.

TEST 20 - WRITE DATA TEST

This test initially writes on and tests five sectors of each diagnostic write track and then performs the same test on the remaining sectors.

TEST 21 - TRANSFER LENGTH TEST

This test carries out a write and read with different transfer lengths between 1 to 32 sectors on a single diagnostic track. The write is a pattern %55 and %AA. Then a read is made first on the two last sectors of the diagnostic cylinder track and then on the first two sectors of the next track. The read and write data is then compared for errors.

TEST 22 - HEAD ALIGNMENT TEST

This test checks the alignment of the heads, by carrying out a series of reads on six read cylinder sectors (one for each track, in the same location).

TEST 23 - ALTERNATIVE TRACK ASSIGNMENT TEST

This test checks the assignment procedures and use of alternative track. Three tracks of the write diagnostic cylinder are filled with different test patterns. These tracks are then assigned with alternative tracks. The alternative tracks are then read and checked for errors.

TEST 24 - ROTATION TIME TEST

This test calculates the mean rotation time using ten speed samples and displays the result. The program will flag out that the rotation time is unacceptable if the rotation time is not is not 16 to 17 ms.

14.1.2 ERROR MESSAGES

TYPE OF ERRORS INDICATED:

- Type A = possible recovery using program
- Type B = possible recovery by operator (ie controller missing)
- Type C = errors which may be due to PU or disk
- Type D = errors which may be due to controller

TYPE A OR C ERRORS it may be necessary to run the VERIFY AND CORRECTION PROGRAM

- ECC on identifiers wrong
- ECC on data field uncorrectible
- Id. address mark not found
- Data address mark not found
- Sector not found
- P.U. positioning on id wrong
- ECC on data correctible error
- Bad block found
- Identifiers test wrong
- Error on altern. track positioning
- Sector out of range
- Multitrack op. error-sect. out of range
- Wrong seek
- Error on reading
- Rotation time un acceptable

TYPE B ERRORS

- No index found on P.U.
- P.U. positioning wrong
- P.U. record circuit fault
- P.U. not ready

- P.U. not selected
- P.U. not on track 0
- More P.U. selected
- Running positioning on P.U.
- Not found present PU

TYPE D ERRORS

- Adapter major error
- Adp/cnt major error
- Adp/cnt anomalous busy
- Controller not selected
- Adp/cnt handshake time-out
- Data verify error
- Lacking controller answer
- Memory error
- Adater interrupt network fault
- Error on adp/cnt handshake time-out
- Error on adp/cnt fast handshake network
- Adapter verify network fault
- Adapter internal busses fault
- Adapter i/o registers or DMA fault
- Adapter timer channel 0 fault
- Adapter timer network fault
- Adapter timer channel 2 fault
- Memory or adp DMA network (data) error
- Memory or adp DMA network (address) error
- Adater DMA memory fault
- Adapter history port fault
- Adapter disconnection fault

- Error for not occured interrupt
- Wrong interrupt occured
- Adp switches position or reading fault
- Adapter type port wrong value
- Unknown FW answer
- Fault on controller ECC network

14.2 C50062: XU5006 CERTIFICATION PROGRAM

PROGRAM PURPOSE

To certify the XU5006 hard disk unit via the SASI3 subsystem.

HARDWARE REQUIRED

XU5006 HDU with DTC510 BP/B0 controller, G0298 and G0299 controller boards.

PRELIMINARY WARNING

This program is intended to be used with disks which do not have an OPE ERMAP in cylinder 305, head 0, i.e. disks which have not been certified by the manufacturer. The program can, however, be used with disks which already have an OPE ERMAP as a new map (OLIVETTI ERMAP) is created with all the errors found.

Certification time : approx. 4.5 Hours.

LOADING PROCEDURE

Refer to section 1.3.2.

14.2.1 TEST DESCRIPTION

The program is subdivided into two phases:

1) Initialization 2) Certification

INITIALIZATION

This phase initializes the adapter and the controller and verifies the compatibility between the adapter, controller and peripheral unit.

CERTIFICATION

Initially the program determines if the disk has been previously certified by OPE or has never been certified.

(i) If the disk has been previously certified by OPE, another error map is created on cylinder 305, head 0, sectors 1 to 3 (sector 0 which contains the OPE error map is left unaltered).

(ii) If the disk has never been certified, an error map of the errors found is compiled on cylinder 305, head 0, sectors 1 to 32.

14.2.2 ERROR MESSAGES

TYPE OF ERRORS INDICATED:

- Type A = possible recovery using program
- Type B = possible recovery by operator (ie controller missing)
- Type C = errors which may be due to PU or disk
- Type D = errors which may be due to controller

ERRORS DUE TO A OR C it may be necessary to run the VERIFY AND CORRECTION PROGRAM

- IDENTIFIER ECC ERROR
- DATA FIELD ECC ERROR
- ID ADDRESS MARK MISSING
- DATA ADDRESS MARK MISSING
- SECTOR NOT FOUND
- POSITIONING ERROR
- RECOVERABLE ECC ERROR
- WRONG TRACK WITHOUT ALTERNATIVE ASSIG.
- BAD ID
- WRONG ALTERNATIVE TRACK
- DATA ERROR DURING VERIFY OPERATION
- REQUESTED "OUT OF RANGE" SECTOR
- ALTERNATIVE TRACK OVERFLOW
- ERROR ON CYLINDER 0
- ERROR ON WRITE DIAGNOSTIC CYLINDER
- ERROR ON READ DIAGNOSTIC CYLINDER
- READ DIAGNOSTIC CYLINDER (304) IS RELOC.
- DEFECTIVE TRACKS OVERFLOW
- DEFECTIVE SECTORS OVERFLOW ON TRACK
- DEFECTIVE TRACKS OVERFLOW ON SURFACE 0/1/2/3/4/5

- ERROR ON R/W LOGICAL
- ERROR IN WRITE PHASE
- ERROR IN READ PHASE
- IDENTIFIER ERROR ON X
- TOO MANY ERRORS (errors > 75)
- TOO MANY ERRORS IN OPE ERMAP (err.>24)
- WRONG ERMAP FIELD
- INPUT OUT OF RANGE! RETYPE!
- *** ERROR IN ERMAP READING ***

TYPE B ERRORS

- PU NOT READY
- PU NOT SELECTED
- TOO MANY PU SELECTED
- PU IN POSITIONING OPERATION
- UNKNOWN CONTROLLER
- PU ABSENT
- UNKNOWN PU

TYPE C OR D ERRORS

- HARDWARE ERROR
- INCOHERENT ANSWER
- I/O ROUTINE TIME OUT
- "ADAPTER" HARDWARE ERROR

14.3 5006F3: XU5006 FORMATTING PROGRAM

PROGRAM PURPOSE

To format the XU5006 hard disk unit via the SASI3 subsystem.

HARDWARE REQUIRED

XU5006 HDU with DTC510 BP/B0 controller, G0298 and G0299 controller boards.

PRELIMINARY WARNING

The disk must be certified by the manufacturer (OPE) or by the OLIVETTI C50062 certification program or by both and must contain at least one error map. Sector 0 of cylinder 305, head 0 is used for the OPE error map and sectors 1 to 3 for the OLIVETTI error map.

Formatting time : approx. 1/2 Hour.

LOADING PROCEDURE

Refer to section 1.3.2.

14.3.1 TEST DESCRIPTION

INITIALIZATION

This phase initializes the adapter and the controller and verifies the compatibility between the adapter, controller and peripheral unit.

FORMATTING

This phase formats the disk surface using the following steps:

a) Reads the OPE and/or the OLIVETTI map on cylinder 305, HD 0.

b) Formats and checks the identifiers, track by track, until all the disk is covered.

c) Assigns alternative user's tracks to the tracks found faulty during the "assalt" procedure (when at least one map is present).

   If there are no faulty tracks on cylinders 303 and 304, these are used respectively for the write and read diagnostic programs.

d) Writes the a series of test patterns, track by track, until all the disk is covered:

14.3.2 ERROR MESSAGES

The error messages are the same as those listed in the corresponding section (11.2.2) of C5006 Certification program.

14.4 ES3564: XU5006 (VIA SASI3) ERROR RATE PROGRAM

PROGRAM PURPOSE

To check the reading and writing operation of an XU5006 hard disk unit when connected to a SASI subsystem and operating under normal user mode.

HARDWARE REQUIRED

XU5006 HDU with DTC510 BP/BO controller, G0298 and G0299 controller boards.

PRELIMINARY WARNING

The write operation in this program destroys data present on the disk. A dump operation should be made before commmencing tests if data is to be preserved.

LOADING PROCEDURES

Refer to section 1.3.2.

14.4.1 TEST DESCRIPTION

GENERAL

WRITE FORWARD (FROM OUTERMOST TO INNERMOST CYLINDER) - TEST 1

Writes test pattern on a number of defined sectors and successively verifies the data written. The test is effected using incremental addressing.

Tests are limited to specific cylinders when cylinder step is NOT 1 and the ALL SURFACES parameter is NOT selected in the pre-program.

WRITE BACKWARDS (FROM INNERMOST TO OUTERMOST CYLINDER)- TEST 2

The test is similar to TEST 1 except that data is written using decremental addressing.

RANDOM WRITE -TEST 3

The test is similar to TEST 1 except that data is written using random addressing.

READ FORWARD (FROM OUTERMOST TO INNERMOST CYLINDER)- TEST 4

Reads the sectors defined in the initial part of the program and if COMPARE DATA is selected, compares the data read with the data in memory used in TEST 1/2. If COMPARE DATA is NOT selected, the data read is checked to see if it corresponds with the ECC value.

The test is carried out using incremental addressing.

READ BACKWARD (FROM INNERMOST TO OUTERMOST CYLINDER)- TEST 5

The test is similar to TEST 4 except that data is read using decremental addressing.

READ RANDOM - TEST 6

The test is similar to TEST 4 except that data is read using random addressing and random transfer lengths (the transfer length entered in the pre-program is ignored). An algorithm is used to generate the cylinder and head ranges and the transfer lengths.

14.4.2 ERROR AND SERVICE MESSAGES

TYPE OF ERRORS INDICATED:

- Type A = possible recovery using program
- Type B = possible recovery by operator (ie controller missing)
- Type C = errors which may be due to PU or disk
- Type D = errors which may be due to controller

ERRORS DUE TO A OR C it may be necessary to run the VERIFY AND CORRECTION PROGRAM

- wrong alternative track
- data field ECC error
- recoverable ECC error
- data error during verify operation
- bad id
- identifier ECC error
- data address mark missing
- id address mark missing
- positioning error
- error on r/w logic

TYPE B ERRORS

- controller absent
- unknown controller
- too much PU selected

- PU absent
- unknown PU
- pu not ready
- pu not selected

TYPE C OR D ERRORS

- hardware error
- incoherent answer
- interrupt unreset

TYPE D ERRORS

- interrupt loop
- adapter unreset
- controller unreset

14.5 SASI24: WRITE STANDARD 24 ON XU5006 (VIA SASI)

PROGRAM PURPOSE

To write STANDARD 24 data on sectors 7 and 12 of track 0, cylinder 0.

HARDWARE REQUIRED

XU5006 HDU with DTC510 BP/BO controller, G0298 and G0299 controller boards.

LOADING PROCEDURES

Refer to section 1.3.2.

14.5.1 TEST DESCRIPTION

The adaptor and controller are initialized and then the data defined by STANDARD 24 is written on sectors 7, 8, and 9 of track 0, cylinder 0 and repeated again on the same track on sectors 10, 11, and 12.

The data contains information on the physical characters on the disk. Refer to the documentation on the STANDARD 24 for detailed information.

14.5.2 ERROR AND SERVICE MESSAGES

TYPE OF ERRORS INDICATED:

- Type A = possible recovery using program
- Type B = possible recovery with the intervention of operator
- Type C = errors which may be due to PU or disk
- Type D = errors which may be due to controller

TYPE A OR C it may be necessary to run the VERIFY AND CORRECTION PROGRAM

- IDENTIFIER ECC ERROR
- DATA FIELD ECC ERROR
- ID ADDRESS MARK MISSING
- DATA ADDRESS MARK MISSING
- SECTOR NOT FOUND
- POSITIONING ERROR

TYPE B ERRORS

- PU NOT READY
- PU NOT SELECTED
- TOO MANY PU SELECTED
- UNKNOWN CONTROLLER
- UNKNOWN PU
- CONTROLLER ABSENT

TYPE C OR D ERRORS

- INCOHERENT ANSWER
- HARDWARE ERROR

ERROR MESSAGES TYPE D

- "ADAPTER" HARDWARE ERROR

SERVICE MESSAGES

- RECOVERABLE ECC ERROR
- WRONG TRACK WITHOUT ALTERNATIVE ASSIG.
- BAD ID
- WRONG ALTERNATIVE TRACK
- DATA ERROR DURING VERIFY OPERATION
- REQUESTED "OUT OF RANGE" SECTOR
- I/O ROUTINE TIME OUT
- ALTERNATIVE TRACK OVERFLOW
- ERROR IN WRITE PHASE
- IDENTIFIER ERROR ON X

14.6 DRSMF4: SAVE/RESTORE XU5006 HDU to XU4305 mFDU TEST PROGRAM

PROGRAM PURPOSE

To evaluate the operation of the two subsystems (SASI3 and mFDU) in alternative and simultaneous operating modes.

HARDWARE REQUIRED

XU5006 HDU with DTC510 BP/B0 controller, G0298 and G0299 controller boards, XU4305 mFDU with G0229, G0280 or G0280/B-D controller.

NOTE

A scratch disk is required.

LOADING PROCEDURES

Refer to section 1.3.2.

14.6.1 TEST DESCRIPTION

GENERAL

The test program comprises a preprogram and an initialization phase and eight main tests which can be selected by the operator.

PREPROGRAM AND INITIALIZING PHASE

The parameters defining system configuration and mode of operation are established. The controllers are identified and initialized.

TEST 1 - WRITE MFLOPPY (4305)

The test comprises writing test pattern "2AAA" on all the MINI FLOPPY sectors, 52 sectors (a cylinder) at a time, regardless of the transfer length entered by the operator. The cylinders will then contain the same pattern except for the first three words of each sector which contain its address (defined by cylinder, head and sector).

The cylinder currently being tested is displayed.

TEST 2 - WRITE DISK (XU5006)

The test comprises writing a test pattern on all the SASI sectors, as in TEST 1 but using the pattern "1555".

The current cylinder, head and sector are displayed together with the total number of sectors used.

TEST 3 - DUMP (alternative cmd)

A number of sectors from the SASI disk as specified by the operator are transfered onto the mFDU using altenative WRITE READ commands.

The current cylinder, head and sector from which the save is made are displayed together with the total number of sectors saved.

TEST 4 - FLOPPY VERIFY

This test checks that the data transferred onto the MINI FLOPPY disk following a dump operation is the same as the original data written on the SASI disk.

The cylinder currently being tested is displayed.

TEST 5 - RESTORE (alternative cmd)

A number of sectors from the mFDU are restored onto the SASI disk using alternative READ WRITE commands.

The current cylinder, head and sector from which the save are made are displayed together with the total number of sectors saved.

TEST 6 - DISK VERIFY

This test checks that the data transferred onto the SASI disk following mFDU restore operation is the same as the data written on the SASI disk.

The current cylinder, head and sector being tested is displayed together with the total number of sectors tested.

TEST 7 - DUMP (overlapped cmd)

This test is similar to the DUMP alternative test except that the READ WRITE commands are issued in overlapped mode.

TEST 8 - RESTORE (overlapped cmd)

This test is similar to the RESTORE alternative test except that the READ WRITE commands are issued in overlapped mode.

14.6.2 ERROR AND SERVICE MESSAGES

The messages are self-explanatory and are listed below.

Change/verify mFDU and/or associated controller for error messages indicated -F-.

Change/verify HDU and/or associated controller for error messages indicated -S- (SASI).

- -F- hardware error/fault/fault recovered

- -F- f.d.c busy
- -F- unknown controller/interrupt
- -F- incoherent answer
- -F- motor ignition fault
- -F- incoherent status
- -F- pu not ready
- -F- write protect
- -F- TIME out error
- -F- error on ID/data field
- -F- DMA overrun
- -F- BAD cylinder
- -F- WRONG cylinder/sector
- -F- missing address on ID/data
- -F- ready change pending
- -S- hardware error!!!
- -S- TIME out error
- -S- p.u. not ready/not selected/in positioning operation !!!
- -S- too much p.u. selected !!!
- -S-identifier ecc error !!!
- -S- data field ecc error !!!
- -S- id address mark missing !!!
- -S- data address mark missing !!!
- -S- sector not found !!!
- -S- recoverable ecc error !!!
- -S- bad id !!!
- -S- data error during verify operation !!!
- -S- requested "out of range" sector !!!
- -S- hardware error !!!

- -S- controller absent !!!
- -S- incoherent answer !!!
- -S- unknown controller !!!
- -S- p.u. absent !!!
- -S- unknown p.u. !!!
- -S- i/o routine time out !!!
- -S- **** abort!!! ****
- error(s) detected in reading/writing/comparing phase
- error on data field
- error on ID/DATA compare
- interrupt loop
- adapter/controller/interrupt unreset

14.7 5006V1: XU5006 HDU VIA SASI3 VERIFY AND CORRECTION PROGRAM

PROGRAM PURPOSE

To display the contents of the HDU data field and condition of disk (no. of faulty tracks, alternative tracks etc.), verify and certify tracks and sectors, and also assign and format alternative tracks.

HARDWARE REQUIRED

XU5006 HDU with DTC510 BP/B0 controller, G0298 and G0299 controller boards.

WARNING

Data is destroyed when certifying or formatting using this program. A dump operation must be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES

Refer to section 1.3.2.

14.7.1 TEST DESCRIPTION

The program provides the following seven functions:

1) Track verify
2) Sector verify
3) Track certify
4) Sector certify
5) Display sector(s)
6) Track processing
7) Disk image

1. Verifies a track with a series of data field reads.

2. Verifies a sector with a series of reads.

3. Certifies a track by performing a series of write and read operations using a default pattern or a pattern entered by the operator.

4. Certifies a sector by performing a series of write and read operations using a default pattern or a pattern entered by the operator.

   The default pattern is a rotating pattern which changes after each write operation as shown in example: DB6D B6DB 6DB6 --> B6DB 6DB6 DB6D --> 6DB6 DB6D B6DB.

5. Displays the data field of one or more sectors in HEX. and ISO characters.

6. Display a MENU from which three operations may be performed:

   a) Check identifier:

   b) Formatting track:

   c) Search first free alternative track:

7. Displays the disk condition, track per track, with the exception of the test track.

14.7.2 SERVICE AND ERROR MESSAGES

TYPE OF ERRORS INDICATED:

- Type A = possible recovery using program
- Type B = possible recovery with the intervention of operator
- Type C = errors which may be due to PU or disk
- Type D = errors which may be due to controller

TYPE B ERRORS

- PU BUSY/NOT READY/IN WRITE PROTECTION CONDITION
- UNKNOWN/ABSENT PU
- PERIPHERAL CONTROL SYSTEM BUSY
- CONTROLLER AND ADAPTER BUSY/ABSENT
- UNKNOWN CONTROLLER
- TOO MANY PU SELECTED

TYPE C OR D ERRORS

- TIME-OUT ERROR
- HARDWARE/SYSTEM/POSITIONING ERROR
- INCOHERENT REPLY

TYPE C ERRORS

- TEMPORARY/ DRIVE FAILURE
- SEEK INCOMPLETE
- BAD/FREE/ASSIGNED ALTERNATIVE TRACK
- GOOD/BAD USER TRACK

- ERROR DURING READ/WRITE PHASE

- ECC/IDENTIFIER/DATA COMPARE/VERIFY/DATA FIELD ECC ERROR:
  ON CYL: xxx HD: xx SECT: xx

- SECTOR NOT FOUND:
  ON CYL: xxx HD: xx SECT: xx

- PU IN POSITIONING OPERATION

- MISSING DATA ADDRESS MARK
  ON CYL: xxx HD: xx SECT: xx

- WRONG TRACK WITHOUT ALTERNATIVE ASSIGN.
  ON CYL: xxx HD: xx

- WRONG ALTERNATIVE TRACK

- MEMORY ERROR

TYPE D ERRORS

- CONTROLLER NOT RESET

14.8 S24X62: WRITE STANDARD 24 ON XU5006 HDU VIA ST506 INTERFACE.

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

XU5006 HDU and G0363 controller.

LOADING PROCEDURE

Refer to section 1.3.2.

14.8.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

a) Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track

b) Recording of the relative part of STANDARD 24 on sector 15.

STANDARD 24 PARAMETERS

Information on sectors 7 to 15, track 0 is obtained by referring to the STANDARD 24 documentation.

Note, the contents given are the initial parameters recorded on the disk. The value of these parameters may have been derived or duplicated from other fields of STANDARD 24.

14.8.2 SERVICE AND ERROR MESSAGES

a) **CONFIGURATION/INITIALISATION ERRORS**

- **PU ABSENT:**

  indicates that the peripheral selected is not connected to the controller.

- **PU NOT READY:**

  re-load the program if error persists or if message appears during program execution the peripheral unit is considered faulty.

- **CONTROLLER INITIALISATION ERROR:**

  the program makes 3 attempts to correct the fault, if the error persists the peripheral unit is considered faulty.

b) **POSITIONING ERRORS**

- **HOME ERROR:**

  this error results when a HOME command is not effected; 5 HOME operations are attempted before the program is aborted.

- **LANDING ZONE POSITIONING ERROR:**

  this error results when the HEAD is not correctly positioned on the LANDING ZONE at the end of the program.

c) **FORMATTING ERRORS**

After formatting the program tests the identifiers of track 0. If errors are found, 3 attempts are made to re-format the track. A HOME operation is performed before each attempt. If the error(s) is not cleared the program is aborted and the following message displayed:

- **ERROR DURING FORMATTING PHASE**

d) **REGISTRATION/CERTIFICATION ERRORS**

- **ERROR DURING WRITING PHASE:**

  displayed after three attempts are made to clear an error detected during writing the complete STANDARD 24 data or only sector 15.

- If after certification, track 0 contains more than 4 defective sectors, the program aborts and a SUMMARY MESSAGE is displayed (see appropriate section).

e) **HARDWARE ERRORS**

One attempt is made to correct the following errors before the error message is displayed and the program aborted.

- **INCOHERENT CONTROLLER RESPONSE**
  HARDWARE ERROR:

  indicates the result of an I/O routine which is not as expected in the program.

- **HARDWARE FAILURE:**

  indicates a general hardware fault.

- **TIME OUT DURING I/O OPERATION**
  HARDWARE ERROR

  indicates time-out error during input/output operations.

- **PU HARDWARE FAILURE:**

  indicates peripheral unit failure.

f) **SUMMARY SERVICE MESSAGES**

The following messages are displayed at the end of the program:

- **STANDARD 24 RECORDED!**
  FIRST USER SECTOR ON TRACK 0 IS XX:

  displayed if the STANDARD 24 has been correctly written or modified on track 0. The sector specified is the first user sector without errors.

- **STANDARD 24 NOT RECORDED!**
  TOO MANY DEFECTIVE SECTORS
  DETECTED ON TRACK 0:

  displayed if more than four defective sectors are found on track 0.

- **ABORT: STANDARD 24 NOT RECORDED:**

  displayed if the program aborts for any reason during execution.

- **PROGRAM NOT EXECUTED!**
  STD 24 ALREADY RECORDED:

  displayed if the operator exits program after detecting that the STANDARD 24 data has already been recorded.

- **SECTOR 15 OF THE**
  STD RECORDED

  displayed if sector 15 of track 0 has been correctly modified.

- **SECTOR 15 OF STD 24 NOT REPLACED!**
  STD 24 NOT ON TRACK 0:

  displayed if during the operation to replace sector 15, STANDARD 24 is NOT found on track 0.

- **ABORT: SECTOR 15 OF**
  STD 24 NOT REPLACED

  displayed if during the operation to replace sector 15, the program aborts.

- **PROGRAM NOT EXECUTED!:**

  displayed if during the operation to replace sector 15, the UNIT NAME and RELEASE fields do not contain the expected data and the operator exits program.

15.1 SM23F6: FUJITSU/SMD3 (XU1700) DISK FORMATTER PROGRAM

PROGRAM PURPOSE

To format the FUJITSU/SMD3 hard disk unit when connected to a SMD3 subsystem.

REQUIRED HARDWARE

FUJITSU/SMD3 hard disk unit (M2312K, 60 Mbytes, single/dual ports), host adaptor SMD3 and controller.

PRELIMINARY WARNING

The disk must be certified by the manufacturer (FUJITSU) and have at least one ermap otherwise formatting is carried out without assigning alternative tracks or initializing the data field.

Also note that any data on the disk before formatting is lost. 22p Formatting time : approx. 1/2 Hour.

LOADING PROCEDURE

Refer to section 1.3.2.

15.1.1 TEST DESCRIPTION

The program comprises the following tests:

1. Identification of the controller and of the subsystem present in the slot positions selected by the operator.

2. Search for defective tracks and certification of the diagnostic tracks and the tracks which contain the ermap.

3. The tracks indicated in the ermap are formatted, excluding the tracks shown in the special data area of the ermap which have been previously considered.

4. Data defined by STANDARD 24 is written on sectors 7 to 12 of cylinder 0, head 0.

5. The diagnostic patterns are written on a reserved cylinder and pattern FFFF on all of the user data field.

15.1.2 ERROR MESSAGES

TYPE OF ERRORS INDICATED:
- TYPE A = errors recoverable using the program
- TYPE B = errors recoverable with the intervention of the operator
- TYPE C = hardware errors which are not recoverable on the PU or dis
- TYPE D = hardware errors which are not recoverable on the controller

ERROR MESSAGES - TYPE A

- NON-RECOVERED ERROR DURING WRITE PHASE

  IDENTIFIER ERROR:
  ID. SOUGHT: XX
  ID. FOUND : XX

- NON-RECOVERED ERROR DURING WRITE PHASE
  DATA ERROR: XX

- NON-RECOVERED ERROR DURING WRITE PHASE
  ECC ERROR: XX

- PERMANENT ERROR DURING WRITE PHASE

  IDENTIFIER ERROR:
  ID. SOUGHT: XX
  ID. FOUND : XX

- PERMANENT ERROR DURING WRITE PHASE
  DATA ERROR: XX

- PERMANENT ERROR DURING WRITE PHASE
  ECC ERROR: XX

- RECOVERED ERROR DURING WRITE PHASE

  IDENTIFIER ERROR:
  ID. SOUGHT: XX
  ID. FOUND : XX

- RECOVERED ERROR DURING WRITE PHASE
  DATA ERROR: XX

- RECOVERED ERROR DURING WRITE PHASE
  ECC ERROR: XX

ERROR MESSAGES - TYPE B

- PU NOT KNOWN
- PU ABSENT OR DOES NOT ACKNOWLEDGE
- PU NOT READY
- OPERATION NOT EXECUTABLE:
  PU IN WRITE PROTECT MODE
- PERIPHERAL CONTROL SYSTEM BUSY

ERROR MESSAGES -TYPE C

- DRIVE IN PERMANENT FAILURE
- DRIVE IN TRANSITORY FAILURE
- UNEXPECTED INTERRUPT RECEIVED FROM
  DRIVE :XX INSTEAD OF DRIVE :YY
- SEEK INCOMPLETE
- ERROR MAP NOT READABLE
  ON CYLINDER XX HEAD YY
- ERROR MAP ON CYLINDER XX HEAD YY
  CONTAINS WRONG DATA
- SEEK INTERRUPT FROM DRIVE NOT USED
- RECOVERED ECC ERROR IN ERMAP SECTORS
- UNRECOVERED ECC ERROR IN ERMAP
  SECTORS XX
- SURFACE ERROR DETECTED DURING TEST PHYSICAL
- RECOVERED POSITIONING ERROR
- UNRECOVERED POSITIONING ERROR
- ERMAP TRACK HAS BEEN WRITTEN BUT
  IT IS NOT POSSIBLE TO READ ALL TRACK
  OFFSET COMBINATIONS
  DATA ON ERMAP NOT READABLE
  PROGRAM ABORTED

- MORE THAN XX
  DEFECTS ON SURFACE YY
  PROGRAM ABORTED

- ERMAP FIELD IS FULL - NO SPACE FOR
  NEW DEFECTS
  PROGRAM ABORTED

- ONLY TWO GOOD IDENTIFIERS ON SECTOR XX

ERROR MESSAGES - TYPE C or D

- TIME OUT ERROR:
  INTERRUPT NOT RECEIVED

- SYSTEM BUS ERROR

- HARDWARE ERROR

- INCOHERENT RESPONSE

- PARAMETER ERROR

ERROR MESSAGES - TYPE D

- READ DATA NOT FOUND IN SYSTEM MEMORY

- NO RESET INTERRUPT IN THE CONTROLLER

NON SPECIFIC ERROR MESSAGE

- SOFTWARE ERROR

15.2 ST2455: WRITE STANDARD 24 ON FUJITSU/SMD3 (XU1700)

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 and 12 of track 0, cylinder 0.

HARDWARE REQUIRED

FUJITSU/SMD3 disk unit (M2312K, 60 Mbytes, dual/single port), host adaptor SMD3 and controller.

LOADING PROCEDURE

Refer to section 1.3.2.

15.2.1 TEST DESCRIPTION

The adaptor and controller are initialized and then the data defined by STANDARD 24 is written on sectors 7, 8, and 9 of track 0, cylinder 0 and repeated again on the same track on sectors 10, 11, and 12.

The data contains information on the physical characters on the disk. A list of the contents on the sectors is shown below. Refer to the documentation on the STANDARD 24 for detailed information.

15.2.2 ERROR MESSAGES

Refer to the ERROR MESSAGES of program ST2455 (section 15.1.2)

15.3 2312E8: FUJITSU/SMD3 (XU1700) ERROR RATE PROGRAM

PROGRAM PURPOSE

To check the reading and writing operation of a FUJITSU/SMD3 disk unit when connected to a SMD3 subsystem and operating under normal user mode.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (M2321K, 60 Mbytes, single/ dual port), host adaptor SMD3 and controller.

LOADING PROCEDURE

Refer to section 1.3.2.

PRELIMINARY WARNING

The write operation in this program destroys data present on the disk. A dump operation should be made before commencing tests if data is to be preserved.

15.3.1 TEST DESCRIPTION

TEST 1 - WRITE & VERIFY FORWARD (NOMINAL)

The test comprises writing a test pattern in nominal mode (without strobe and track offset) on all the sectors of a defined cylinder range and head and successively verifying (between disk and controller) the data written. The test is effected using incremental addressing and in steps of a defined number of sectors until all the required sectors are tested.

TEST 2 - WRITE & VERIFY FORWARD (MARGINATED)

The test comprises writing a test pattern in marginated mode (with strobe and track offset) on all the sectors of a defined cylinder range and head. The data written is verified four times (between disk and controller), each time varying the strobe (early/late)and the track offset (plus/minus). The test is effected using incremental addressing and in steps of a defined number of sectors until all the required sectors are tested.

TEST 3 - WRITE & VERIFY BACK (NORMAL)

The test is similar to TEST 1 except that data is written using decremental addressing.

TEST 4 - WRITE & VERIFY BACK (MARGINATED)

The test is similar to TEST 2 except that data is written using decremental addressing.

TEST 5 - READ FORWARD (NOMINAL)

This test is similar to Test 1 except data is readin nominal mode as opposed to being written.

TEST 6 - READ FORWARD (MARGINATED)

This test is similar to Test 2 except data is read in marginated mode as opposed to being written.

TEST 7 - READ BACK (NORMAL)

The test is similar to TEST 1 except that data is read (as opposed to written) using decremental addressing.

TEST 8 - READ BACK (MARGINATED)

The test is similar to TEST 2 except that data is read using decremental addressing.

TEST 9 - READ RANDOM (NORMAL)

The test is similar to TEST 1 except that data is read (as opposed to written) using random addressing.

TEST 10 - READ RANDOM (MARGINATED)

The test is similar to TEST 2 except that data is read (as opposed to written) using random addressing.

15.3.2 ERROR MESSAGES

Refer to the ERROR MESSAGES of program SM23F6 (section 15.1.2) plus the following.

TYPE OF ERRORS INDICATED:
- TYPE A = errors recoverable using the program
- TYPE B = errors recoverable with the intervention of the operator
- TYPE C = hardware errors which are not recoverable on the PU or disk
- TYPE D = hardware errors which are not recoverable on the controller

ERROR MESSAGES - TYPE A

- NON-RECOVERED ERROR DURING WRITE /READ PHASE
  IDENTIFIER ERROR:
  ID. SOUGHT: XX
  ID. FOUND : XX

- NON-RECOVERED ERROR DURING WRITE/READ PHASE
  DATA ERROR: XX

- NON-RECOVERED ERROR DURING WRITE/READ PHASE
  ECC ERROR: XX

- PERMANENT ERROR DURING WRITE PHASE
  IDENTIFIER ERROR:
  ID. SOUGHT: XX
  ID. FOUND : XX

- PERMANENT ERROR DURING WRITE/READ PHASE
  DATA ERROR: XX

- PERMANENT ERROR DURING WRITE/READ PHASE
  ECC ERROR: XX

- RECOVERED ERROR DURING WRITE PHASE
  NO. OF ATTEMPTS: XX
  IDENTIFIER ERROR:
  ID. SOUGHT: XX
  ID. FOUND : XX

- RECOVERED ERROR DURING WRITE/READ PHASE
  NO. OF ATTEMPTS: XX
  DATA ERROR: XX

- RECOVERED ERROR DURING WRITE/READ PHASE
  NO. OF ATTEMPTS: XX
  ECC ERROR: XX

ERROR MESSAGES - TYPE C or D

- MAIN MEMORY DATA COMPARE ERROR
  HARDWARE FAILURE:
  ALL DATA NOT TRANSFERRED

- MAIN MEMORY DATA COMPARE ERROR
  HARDWARE FAILURE:
  SOME DATA NOT TRANSFERRED

- MAIN MEMORY DATA COMPARE ERROR:
  HARDWARE FAILURE:
  WRONG DATA TRANSFERRED

- MAIN MEMORY DATA COMPARE ERROR:
  HARDWARE FAILURE:
  WRONG BLOCK LABEL FOUND

15.4 23SCT3: FUJITSU (XU1700)/SMD3 and STC SAVE-RESTORE PROGRAM

PROGRAM PURPOSE

To evaluate the error rate of the FUJITSU/SMD3 subsystems and the STC subsystem by writing and reading sample patterns under critical conditions and performing SAVE (disk to tape) and RESTORE (tape to disk) operations.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (XU 1700/M2312K, 60 Mbytes, single/dual ports), SMD3 adaptor and controller, streaming tape cartridge unit (STC), STC adaptor and controller.

PRELIMINARY WARNING

The write, save and restore operations in this program destroys data present on both disk and tape units. A dump operation on each unit should be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES

Refer to section 1.3.2.

15.4.1 TEST DESCRIPTION

GENERAL

There are 10 tests/operations which can be selected by the operator. For the HDU the operator defines the cylinder range, head, the number of sectors to be operated on at a time (steps) and the number of times the test is to be repeated (cycles). For the TAPE the operator defines the track range, the number of blocks to be operated on at a time and the number of times the test is to be repeated. The tests are described below.

1) WRITE HDU

The test comprises writing a test pattern which increments from %0000 to %7FFF on the HDU.

2) READ HDU

In this test, the HDU is read and the data read compared in memory with the data originally used for writing on the tape. For this reason it is important to perform operations in the following order: erase the tape, write on tape, restore data from tape to HDU and then read HDU.

3) WRITE TAPE

The test comprises writing a test pattern which decrements from %FFFF to %8000 on the tape. A write operation must always follow a tape erase operation.

4) READ TAPE

In this test, the tape is read and the data read compared in memory with the data originally used for writing on the disk. For this reason it is important to perform operations in the following order: erase tape, write on HDU, save data from HDU to tape and finally read tape.

5) HDU --> TAPE

The test comprises a save operation in which data is transferred from HDU to tape in overlapped mode (after each transfer the data is verified). Before each transfer the memory is erased by a cancellation pattern %AAAA.

6) TAPE --> HDU

The test comprises a restore operation in which data is transferred from the tape to the HDU in overlapped mode. Before each transfer the memory is erased by a cancellation pattern %5555.

7) PRECOND TAPE

The operation permits the tape to be pretensioned.

8) REWIND TAPE

The rewind operations are carried out automatically by the program but can be introduced in the test sequence if required.

9) ERASE TAPE

The erase operation can be introduced in the test sequence if required.

10) PAUSE

The pause operation can be introduced in the test sequence if require (to cool the tape unit).

15.4.2 ERROR MESSAGES

TYPE OF ERRORS INDICATED:
- TYPE A = errors recoverable using the program
- TYPE B = errors recoverable with the intervention of the operator
- TYPE C = hardware errors which are not recoverable on the PU or disk/tape
- TYPE D = hardware errors which are not recoverable on the controller

NOTE: If the display has not changed for 10 seconds, the following message is displayed: TIMEOUT: X' X" TIME Y' Y" (where: X' X" = default value and Y' Y" = time taken between displays).

HDU MESSAGES

ERROR MESSAGES - TYPE A

HDU ERROR DETECTED:

- ERROR DETECTED DURING WRITE/READ PHASE:

  IDENTIFIER ERROR:
  ID SOUGHT: FB = %XX, CLY = CC, HD = H, SEC = SS
  ID FOUND: FB = %XX, CLY = CC, HD = H, SEC = SS

- ERROR DETECTED DURING WRITE/READ PHASE:
  DATA ERROR: FB = %XX, CLY = CC, HD = H, SEC = SS

- ERROR DETECTED DURING WRITE/READ PHASE:
  ECC ERROR: FB = %XX, CLY = CC, HD = H, SEC = SS

ERROR MESSAGES - TYPE B

- PU NOT KNOWN

- PU ABSENT OR DOES NOT ACKNOWLEDGE

- PU NOT READY

- OPERATION NOT EXECUTABLE:
  PU IN WRITE PROTECT MODE

- PERIPHERAL CONTROL SYSTEM BUSY

ERROR MESSAGES -TYPE C

HDU ERROR DETECTED:

- DRIVE IN PERMANENT FAILURE

- DRIVE IN TRANSITORY FAILURE

- UNEXPECTED INTERRUPT RECEIVED FROM
  DRIVE :XX INSTEAD OF DRIVE :YY

- SEEK INCOMPLETE

ERROR MESSAGES - TYPE C or D

- TIME OUT ERROR:
  INTERRUPT NOT RECEIVED

- SYSTEM BUS ERROR

- HARDWARE ERROR

TAPE MESSAGES

ERROR MESSAGES - TYPE A

TAPE ERROR DETECTED:

- ERROR DURING WRITE/READ PHASE:
  CARTRIDGE CRASH
- ADDRESS NOT ALIGNED

ERROR MESSAGES - TYPE B

TAPE ERROR DETECTED:

- OPERATION NOT EXECUTABLE:
  PU IN WRITE PROTECT MODE
- STC SYSTEM BUSY
- CARTRIDGE NOT INSERTED
- WRITE ATTEMPTED ON TRACK NOT ERASED
- INTERRUPTION BY OPERATOR

ERROR MESSAGES -TYPE C or D

TAPE ERROR DETECTED:

- HARDWARE ERROR
- UNEXPECTED EOT DETECTED (EOT = END OF TAPE)

ERROR MESSAGE - TYPE D

- MEMORY TRANSFER FAULT
- ONE BUFFER NOT TRANSFERRED

NON SPECIFIC ERROR MESSAGE

- SOFTWARE ERROR

15.5 SM0611: SMD CONTROLLER (FOR XU1700) DIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To test the SMD3 adaptor and controller when connected to 1, 2, 3 or 4 FUJITSU/SMD3 hard disk units.

REQUIRED HARDWARE

FUJITSU/SMD3 hard disk unit (M2312K/XU 1700, 589 cylinder, 60 Mbytes, single/dual ports), SMD3 adaptor and controller.

WARNING

The disk units connected to the SMD3 adaptor, which are not included in the test, may be left connected and ON LINE but must not be selected for the READ/WRITE test.

Cylinder 587 is reserved for the diagnostic tests. The cylinder must be formatted and must contain an OLIVETTI test program.

Cylinder 586 track 06 must not contain any errors.

NOTE

The tests 1 to 26 must be carried out sequentially with the exception of tests 15 to 16 which may be omitted if the following conditions are present:

-test 15 ; the RAM size is not known and the test gives an error,

-test 16 ; the reserved test cylinder is faulty.

LOADING PROCEDURES

Refer to section 1.3.2.

15.5.1 TEST DESCRIPTION

TEST 1

Checks if the SMD3 controller is in its correct slot position as selected by the operator.

TEST 2

Checks the decoding circuit of the CONFA signal which enables a preprogrammed constant. This constant is used to identify the controller by testing the board identifier switch setting. The switch setting can be changed and tested during the test.

TEST 3

Checks the selection and decoding circuits associated with the generation and reading of the RESEB signal.

TEST 4

Checks the circuits which generate the PRINO signal, interrupts and associated vectors.

TEST 5

Checks the circuits which generate and control the two OFFS (positioning) signals.

TEST 6

Checks channels 1 and 2 of the 8253 and associated components in timer mode, by verifying that the time out period is within tolerance.

TEST 7

Checks the DMA logic by initially transferring a block of 8 words between the DMA and the RAM and then checking the transmission time, the generation of the appropriate interrupt and the enabling/disabling signals. Further transfers are then made with an increasing number of words in each block using the signal EDVE to check the transmission time (LONG, EDVE = 0, SHORT, EDVE = 1).

TEST 8

Checks the read/write logic and addressing of the "4x4 register" files, and the decoding circuit of the EICCA signal.

TEST 9

Performs the same tests as described in test 8 with the exception that signal EILCA is tested instead of signal EICCA.

TEST 10

Checks the decoding circuit of the LOSEA signal which is used for loading (in parallel) the sector counter, and also the decoding circuit of the ESECA signal which is used to read the output of the same counter.

TEST 11

Checks the circuits used for decoding signals INBEP, RESLA and RESHA which enable the input gates to be read. The test also checks the positioning signals ROUT1/2, BECOO, RESK 1, 2, 3, 4 etc. which are memorised using the decode of signals LCOMC and LCOMB.

TEST 12

Checks the decoding circuit for the signal UST00 which is used to load the peripheral name (DIKW0, NOME0/1/2) and the signal REUSA which is used to read the reply to the peripheral selection (UNSD 1-2-3-4).

TEST 13

Checks the circuit which generates the disk error signal FOLT0 and the circuit which reads the FOLT0 signal using FLAGA/REDKA.

TEST 14

Checks the presence of driver 0 and, if ON LINE selects a peripheral and sends a positional command to cylinder 1 using bits 00/19 loaded from DIKW0 and confirmed by SETA1. The test also checks the interrupt generated, the PRIN0 signal and the relative SKER0 signal from the REUSA gate.

The test is carried out on the SEEK generators of all four drivers.

TEST 15

Tests the DMA logic which selects the transfer of data, segment by segment, from the RAM, limiting the test to the free memory area.

TEST 16

Initially the driver selected is set to make a physical read of a sector, then the three identifier groups and successive characters 0000E0 are read and tested.

When making a physical read only the 8235 component is used for generating the interrupt after reading 298 bytes of the sector. The ROM components, the synchronization circuit of the data field and the comparator circuit of the three identifiers (4x4 register file and sector counter) are not used.

TEST 17

The identifier and the sector to be read is loaded and tested using the 4x4 register file and the input of the error status gate RIERA. A test is then made to force an error (a change of 1 or more bits) in the 4x4 register to see if the error is detected between the data contained in the register and the data read from the disk.

TEST 18

Checks the identifiers and verifies if the correct head positioning has been selected.

TEST 19

Reads the sectors of the read only cylinder and tests the data field byte per byte.

TEST 20

Tests the logic which reads the consecutive sectors using the values left on the sector gates (i.e. tests the sector counter).

TEST 21

Tests the identifiers of the user cylinder and the generation of an error signal (SKERO) when a cylinder not present (other than cylinder 589) is selected.

TEST 22

Compares the 256 bytes of the RAM board with the data registered on the sector and verifies that the data is the same.

TEST 23

Forces a change of bits in the RAM and verifies using test 22 that an error is signalled.

TEST 24

Tests the BURST ERROR PROCESSING circuit which corrects errors and indicates when errors can or cannot be corrected between data in RAM and data on a sector. The test is carried out using comparator circuits and by counting the number of clock pulses needed to correct each of the four internal registers.

TEST 25

Tests the circuit used for recording a sector.

TEST 26

Checks the sector formatting logic and the logic which detects identifier errors by forcing identifier errors during formatting and verifying the following:

- when 2 out of 3 groups of identifiers are different the data field is not read and the error is signalled.
- when 1 out of 3 groups of identifiers is different the data field is read and the error signalled.

15.5.2 ERROR MESSAGES

The following messages are provided:

N.8. Where indicated : (1) = Probable Controller error,
(2) = Probable SMD3 Adapter error,
(3) = Probable Controller or Adapter error (test with disk).

Also XXXX, YYYY, ZZZZ, VVVV, WWWW = data unless otherwise indicated.

GENERAL:

-CONTROLLER/FORMATTER BOARD FAULT

-THIS TEST USES THE DRIVER

TEST 1: -ANSWER TO BOARD TYPE IS FF

(1) -BOARD TYPE NOT AS EXPECTED
OLIBUS SIGNAL READ BY INPUT INSTR.
TIPON
XXXX STUCK AT 0 OR 1
XXXX = faulty signal on output of TIPON gate (BDA00 - BDA07)

-8 BIT +SIGNIF. DATA-BUS DOES NOT = FF

-AT ADDRESS XXX SELECT BOARD TYPE =YY

-IND10=0 SELECT BOARD TYPE

-IND60=0 SELECT BOARD TYPE

-BOARD TYPE IS OUTPUT EVEN DURING RESET

-BOARD IS NOT PRESENT IN THIS SLOT

-1AD30=0 SELECT BOARD TYPE

-NO SUCH SLOT POSITION
VERIFY IF BOARD IS IN ASSIGNED SLOT

TEST 2: -SWITCH CONFIGURATION FOUND = FF

(1) -SWITCH CONFIG. WRONG BIT : XXXX
OLIBUS SIGNAL READ BY INPUT INSTR.
CONFA
XXXX STUCK AT 0 OR 1
XXXX = faulty signal on output of CONFA gate (DK001 - DK151)

```
TEST 3:     -FLAGA INPUT ANSWER = FF

 (1)        -SIGNALS ERROR ON PORT
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       FLAGA
             XXXX STUCK AT 0 OR 1
             XXXX = faulty signal on output of FLAGA gate (FOLTO, ERBU1,
                    PAERO, RESEB, PRINO).

            -SIGNAL RESEB NOT 1

            -SIGN.RESEB NOT 0 AFTER OUTPUT = 0

            -SIGN.ABCON NOT DISABLED BY PORES

            -SIGN.ABCON STUCK AFTER I/O TIPON

            -SIGN.RESEB = 1 AFTER PORES RESET

TEST 4:     -CHECK VECTORS : FIRST INTERRUPT
 (1)         SIGNAL PRINO NOT 1 AFTER GEINO = 1

            -CHECK VECTORS : FIRST INTERRUPT
             ERROR ON INTERRUPT VECTOR
            -OLIBUS SIGNAL READ BY INPUT INSTR.
                       OLIBUS
             XXXX STUCK AT 0 OR 1
             XXXX = faulty signal on OLIBUS (BDA00 - BDA07)

            -CHECK VECTORS : FIRST INTERRUPT
             DURING INTERRUPT, GEINO & ENIRO NOT 1

            -CHECK VECTORS : FIRST INTERRUPT
             WHEN PORES = 0 INT. REQ.DOES NOT EXIT

            -CHECK VECTORS : FIRST INTERRUPT
             INTERRUPT EXIT WHEN GEINO=1 ENIRO=0

            -CHECK VECTORS : FIRST INTERRUPT
             INTERRUPT OCCURS DURING INT.PENDING

            -CHECK VECTORS : FIRST INTERRUPT
             PRINO NOT 0 WHEN GEINO=0

            -CHECK VECTORS : FIRST INTERRUPT
             PRINO NOT 0 WHEN PORES RESET
```

```
TEST 5:     -INPUT REDKA WRONG READ = FF

 (1)        -INPUT REDKA TEST BIT OFFS0-OFFS1
             OLIBUS SIGNAL READ BY INPUT INSTR.
                    REDKA
             XXXX STUCK AT 0 OR 1
             XXXX = faulty signal on output of REDKA gate (SKERO, FOLTO,
                    BUSEO, WRIP2, ONTRO, UNRYO, OFFS0, OFFS1)

            -INPUT REDKA NOT 00 AFTER RESET

TEST 6:     -IN530 AT 1 AFTER 8253 PROGR.

 (1)        -ENTIO=1 NO CLOCK FOR 8253-IN530 = 0

            -SIGNAL PRINO LATE TO EXIT

            -WITH ENTIO=0  ZOLU1-PRINO=1

            -WHEN 8253 HAS HIGH TIME VALUE:PRINO=0

            -8253 TIMER TIME TOO FAST XXXX

            -8253 TIMER TIME TOO SLOW XXXX

            -CLOCK NUMBER FOR 8253 AT 2MHZ=

            -THE SYSTEM CLOCK IS 1.2307 MHZ

            -COUNT. REACHED 0 BEFORE CLOCKS

            -COUNT. REACHED 0 AFTER CLOCKS

TEST 7:     -SIGNAL PRINO NOT 1 : NO DMA
(1)        * OLIBUS SIGNAL READ BY INPUT INSTR.
           *            FLAGA
         # *   XXXX STUCK AT 0 OR 1
           *   XXXX = faulty signal on output of FLAGA gate
           *          (FOLTO, ERBUI, PAERO, RESEB, PRINO)

            -PRINO NOT 0 WHEN DMARO=1 LUINO=0
                   (same # above)

            -PRINO 0=0 LUINO=0
                   (same #)

            -PRINO NOT 1 WHEN DMARO=1 LUINO=1
                   (same #)

            -AFTER REPROGR.8253 PRINO NOT 1
                   (same #)
```

```
        -3 BLOCKS DMA TRANSF. -PRINO NOT 1
               (same #)

        -ENDRO=0:DMA ERR. FOR PRINO NOT 0
               (same #)

        -3FF DMA BLOCKS WITH EDVE1=1 -PRINO=0
               (same #)

        -3FF DMA BLOCKS WITH EDVE1=0 -PRINO=0
               (same #)

        -START DMA WITH RESEB=0:PRINO NOT 0
               (same #)

        -DMA FOR GENER. SIGNAL ERBUI - SEGM.00
               (same #)

        -EDVE1=0 TRANSF. TIME > EXPECTED
      * DMA FROM SYSTEM RAM TO BOARD RAM
      * LOGIC ADDRESS-WORD XXXX
   ## * PHYSICAL ADDRESS-BYTE  XXXX
      * CORRECT WAITING TIME XXXX
      * TIME TAKEN XXXX

        -EDVE1=0 TRANSF. TIME < EXPECTED
               (same ##)

        -EDVE1=1 TRANSF. TIME > EXPECTED
               (same ##)

        -EDVE1=1 TRANSF. TIME < EXPECTED
               (same ##)

        -ERROR ON DATA TRANSFER
      *  DMA FROM SYSTEM RAM TO BOARD RAM
      *  LOGIC ADDRESS-WORD XXXX
      *  PHYSICAL ADDRESS-BYTE XXXX
      *  DMA CYCLES (8 WORD) IN TRASM.  XXXX
      *  VALUE WRITTEN IN DMA RAM XXXX
  ### *  DMA FROM BOARD RAM TO SYSTEM RAM XXXX
      *  LOGIC ADDRESS-WORD XXXX
      *  PHYSICAL ADDRESS-BYTE XXXX
      *  DMA CYCLES (8 WORD) IN TRASM. XXXX
      *  DATA RD FROM BOARD TO DMA RAM XXXX
      *  ADDRESS RAM FAULT (WORD) XXXX
      *  ADDRESS RAM FAULT (BYTE) XXXX

        -ERR. TRANSF.DMA > MAX ADDRESS
               (same ###)
```

```
                -1FF BLOCKS TRANSF.:ERROR ON DATA
                      (same ###)

                -1FF BLOCKS TRANSF.: OVERFLOW ERROR
                      (same ###)

                -TEST 8K RAM - YY=55
                      (same ###)

                -ERROR ON FIRST CELL AFTER 8K
                      (same ###)

                -TEST 8K RAM - YY=AA
                      (same ###)

                -TRANSF. 8K +1 WORD - WORD 0 NOT MODIFIED
                      (same ###)

                -ALGORITHM: HADD XOR LADD XOR YY
                 (HADD = most significant address,
                  LADD = least significant address,
                  XOR  = function)

TEST 8:         -INPUT READ WITH EICCA, FAILED =FF
              *  OLIBUS SIGNAL READ BY INPUT INSTR.
 (2)          *             EICCA
              *  XXXX STUCK AT 0 OR 1
    ####      *  XXXX = faulty signal on output of EICCA gate
              *        (DAC00 -DAC07)
                 VALUE WRITE - ADDRESS - VALUE READ
                     WWWW       YYYYY      ZZZZ

                -FIRST CHECK EXECUTED ON CIRCUIT
                 4 BIT INPUT REGISTER FILE EICCA
                      (same ####)

                -SECOND CHECK EXECUTED ON CIRCUIT
                 4 BIT INPUT REGISTER FILE EICCA
                      (same ####)

                -SECOND CHECK EXECUTED ON CIRCUIT
                 4 BIT INPUT REGISTER FILE EICCA
                -ERROR ON ADDRESSING REGISTERS
                      (same ####)

TEST 09         -INPUT READ WITH EILCA,FAILED =FF
              * OLIBUS SIGNAL READ BY INPUT INSTR.
 (2)          *             EITRA
              *  XXXX STUCK AT 0 OR 1
    #####     *  XXXX = faulty signal on output of EITRA gate
              *        (DAC00 -DAC07)
                 VALUE WRITE - ADDRESS - VALUE READ
                     WWWW       YYYYY      ZZZZ
```

```
            -FIRST CHECK EXECUTED ON CIRCUIT
             4 BIT INPUT REGISTER FILE EILCA
                    (same #####)

            -SECOND CHECK EXECUTED ON CIRCUIT
             4 BIT INPUT REGISTER FILE EILCA
                    (same #####)

            -SECOND CHECK EXECUTED ON CIRCUIT
             4 BIT INPUT REGISTER FILE EILCA
             ERROR ON ADDRESSING REGISTERS
                    (same #####)

TEST 10     -INPUT READ WITH ESECA,FAILED =FF
            FIRST CHECK EXECUTED ON CIRCUIT
 (2)
            -FIRST CHECK EXECUTED ON CIRCUIT
             INPUT PORT ESECA :BITS FAILED

            -SECOND CHECK EXECUTED ON CIRCUIT
             INPUT PORT ESECA :BITS FAILED

TEST 11     -OUTPUT LCOMB,INPUT INBEP: READ FF
            FIRST CHECK EXECUTED ON CIRCUIT
 (2)
            -OUTPUT LCOMB,SIGNALS BECXO/BECOO
             FIRST CHECK EXECUTED ON CIRCUIT

            -OUTPUT RESET,SIGNALS BECXO/BECOO

            -OUTPUT LCOMC,SIGNALS ROUT1/ROUT2

            -OUTPUT LCOMC,INPUT INBEP: READ FF

            -OUTPUT RESET,SIGNALS ROUT1/ROUT2

            -OUTPUT LCOMC,SIGNALS RESK1/2/3/4

            -FIRST CHECK EXECUTED ON CIRCUIT
             OUTPUT RESET,SIGNALS RESK1/2/3/4

            -FIRST CHECK EXECUTED ON CIRCUIT

TEST 12:    -DRIVE 0 SELECTION - CHECK UNSD1
          * OLIBUS SIGNAL READ BY INPUT INSTR.
 (2)      *          REUSA
        @ *  XXXX STUCK AT 0 OR 1
          *  XXXX = faulty signal on output of REUSA gate
          *         (UNS01 - UNS02, SKE1A - SKE4A)

            -DRIVE 0 SELECT.-SIGNALS MODIFIED:
                    (same @)

            -AFTER RESET DRIVE 0 ALWAYS SELECTED.
                    (same @)
```

-DRIVE 2 SELECTION - CHECK UNSD2
(same @)

-DRIVE 2 SELECT.-SIGNALS MODIFIED:
(same @)

-AFTER RESET DRIVE 2 ALWAYS SELECTED.
(same @)

-DRIVE 4 SELECTION - CHECK UNSD3
(same @)

-DRIVE 4 SELECT.-SIGNALS MODIFIED:
(same @)

-AFTER RESET DRIVE 4 ALWAYS SELECTED.
(same @)

-DRIVE 6 SELECTION - CHECK UNSD4
(same @)

-DRIVE 6 SELECT.-SIGNALS MODIFIED:
(same @)

-AFTER RESET DRIVE 6 ALWAYS SELECTED.
(idem @)

-DRIVE OFF/LINE SIGNAL NOMEO/1/2= XXXX

-UNSDX=1 BEFORE INPUT CLOCK UST00
(same @)

TEST 13: -AFTER RESET FOLTO=1,PORT FLAGA

(2) -AFTER RESET FOLTO=1,PORT REDKA

-GENERAT. SIGNAL FOLTO(FOLTO=1)
SIGNAL FOLTO=1 ON REDKA BUT=0 ON FLAGA

-GENERAT. SIGNAL FOLTO(FOLTO=1)
SIGNAL FOLTO=0 ON REDKA BUT=1 ON FLAGA

-GENERAT. SIGNAL FOLTO(FOLTO=1)
SIGNAL FOLTO=0 ON REDKA AND FLAGA

-GENERAT. COMMAND RESET FOLTO
SIGNAL FOLTO=1 ON REDKA BUT=0 ON FLAGA

-GENERAT. COMMAND RESET FOLTO
SIGNAL FOLTO=0 ON REDKA BUT=1 ON FLAGA

```
            -GENERAT. COMMAND RESET FOLTO
             SIGNAL FOLTO=1 ON FLAGA AND REDKA

            -SIGNAL FAILED AFTER RESET BOARD/DRIVE
             OLIBUS SIGNAL READ BY INPUT INSTR.
                      REDKA
               XXXX STUCK AT 0 OR 1
               XXXX = faulty signal on output of REDKA gate (SKER0, FOLTO,
                      BUSE0, WRIP2, ONTR0, UNRY0, OFFS0, OFFS1)

            -GENERAT. SIGNAL FOLTO(FOLTO=1)
             SIGNAL FAILED WITH SIGNAL RESEB = 1

TEST 14:    -RESET/FOLTO SEEK SETA0 CLK CYL.1
          * OLIBUS SIGNAL READ BY INPUT INSTR.
          *          FLAGA
       @@ *  XXXX STUCK AT 0 OR 1
          *  XXXX = faulty signal on output of FLAGA gate (FOLTO,
          *         ERBUI, PAER0, RESEB, PRIN0)

            -EISK1=0 DISAB.SKEM1 X SKE1A = 1
                      (same @@)

            -EISK1/4=1 ENABLE JK WITH SENDX CLK
                      (same @@)

            -RESK1=0 FOR RESET JK: SIGNAL SKEM1
                      (same @@)

            -EISK2=0 DISAB.SKEM2 X SKE2A = 1
                      (same @@)

            -RESK2=0 FOR RESET JK: SIGNAL SKEM2
                           (same @@)

            -EISK3=0 DISAB.SKEM3 X SKE3A = 1
                      (same @@)

            -RESK3=0 FOR RESET JK: SIGNAL SKEM3
                      (same @@)

            -EISK4=0 DISAB.SKEM4 X SKE4A = 1
                      (same @@)

            -RESK4=0 FOR RESET JK: SIGNAL SKEM4
                      (same @@)
```

```
     -RESET/FOLTO SEEK SETAO CLK CYL.1
     * OLIBUS SIGNAL READ BY INPUT INSTR.
     *            REUSA
@@@  *  XXXX STUCK AT 0 OR 1
     *  XXXX = faulty signal on output of REUSA gate
     *         (UNS01 - UNS04, SKE1A - SKE4A)

     -EISK1=0 DISAB.SKEM1 X SKE1A = 1
              (same @@@)

     -EISK1/4=1 ENABLE JK WITH SENDX CLK
              (same @@@)

     -RESK1=0 FOR RESET JK: SIGNAL SKEM1
              (same @@@)

     -REPOSIT.WITH SEEK SIGNAL SKE1A
              (same @@@)

     -AFTER RESET,BUT NO CLOCK SENDX
              (same @@@)

     -AFTER RESET,ENABLE JK EISK1
              (same @@@)

     -EISK2=0 DISAB.SKEM2 X SKE2A = 1
              (same @@@)

     -RESK2=0 FOR RESET JK SIGNAL SKEM2
              (same @@@)

     -REPOSIT.WITH SEEK SIGNAL SKE2A
              (same @@@)

     -AFTER RESET,ENABLE JK EISK2
              (same @@@)

     -EISK3=0 DISAB.SKEM3 X SKE3A = 1
              (same @@@)

     -RESK3=0 FOR RESET JK SIGNAL SKEM3
              (same @@@)

     -REPOSIT.WITH SEEK SIGNAL SKE3A
              (same @@@)

     -AFTER RESET,ENABLE JK EISK3
              (same @@@)

     -EISK4=0 DISAB.SKEM4 X SKE4A = 1
              (same @@@)
```

```
                -RESK4=0 FOR RESET JK SIGNAL SKEM4
                         (same @@@)

                -REPOSIT.WITH SEEK SIGNAL SKE4A
                         (same @@@)

                -AFTER RESET,ENABLE JK EISK4
                         (same @@@)

                -RESK1/4=1 EISK1=1 NO SEEK/SENDX
                         (same @@@)

TEST 15:        -TRANSFER ADDRESS DMA = XXXX
                 ADDRESS RAM FAULT (WORD)  XXXX
 (2)             CRT.EXPECTED XXXX
                 CRT.FOUND    XXXX

TEST 16:        -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :4 REG.FILE CHANGED
 (2)           * CRT.EXPECTED XXXX
     @@@@      * CRT.FOUND    XXXX

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :FIRST WORD = FLAG/CYL+
                       (same @@@@)

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :SECOND WORD = CYL-/HEAD
                       (same @@@@)

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :THIRD WORD READ=SECTOR
                       (same @@@@)

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :SECOND IDENTIFIER
                       (same @@@@)

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :THIRD IDENTIFIER
                       (same @@@@)

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :SYNC. IDENTIF.
                       (same @@@@)
```

```
                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :STATUS PORT CHANGED
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          RIERA
                 XXXX STUCK AT 0 OR 1
                 XXXX = faulty signal on output of RIERA gate (ERP01, ERDA1,
                        ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

                -FIRST 40 BYTE SECTOR -PHYSICAL READ XXXX
                 PHYSICAL READ :NOT SYNCHRONISED

TEST 17:        -IDENTIF.ERROR
                 FLAG CHECK
 (3)           * IDENTIF.CYL. READ  0C024B0001 XXXX
               * OLIBUS SIGNAL READ BY INPUT INSTR.
    @@@@@      *          EITRA
               * XXXX STUCK AT 0 OR 1
               * XXXX = faulty signal on output of EITRA gate (DAC00 -DAC07)

                -IDENTIF.ERROR
                 CYL. + SIGNIF.
                          (same @@@@@)

                -IDENTIF.ERROR
                 CYL. - SIGNIF.
                          (same @@@@@)

                -IDENTIF.ERROR
                 HEADER READ
                          (same @@@@@)

                -IDENTIF.ERROR
                 SECTOR
                 IDENTIF.CYL. READ  0C024B0001 XXXX
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          ENSEA
                 XXXX STUCK AT 0 OR 1
                 XXXX = faulty signal on output of ENSEA gate (CSE00 -CSE07)

                -STATUS PORT TO IDENTIF.
                 IDENTIF.CYL. READ  0C024B0001 XXXX
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          RIERA
                 XXXX STUCK AT 0 OR 1
                 XXXX = faulty signal on output of RIERA gate (ERP01, ERDA1,
                        ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

                -SIGNAL PORT PRIN0=INTERRUPT
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          FLAGA
                  XXXX STUCK AT 0 OR 1
                  XXXX = faulty signal on output of FLAGA gate (FOLT0,
                         ERBUI, PAERO, RESEB, PRIN0)
```

```
TEST 18:    -IDENTIF.ERROR
             HEADER READ  XXXX
 (3)         HEAD  - SECTOR EXPECTED XXXX
           *  OLIBUS SIGNAL READ BY INPUT INSTR.
         $ *            EITRA
           *  XXXX STUCK AT 0 OR 1
           *  XXXX = faulty signal on output of EITRA gate (DAC00 -DAC07)

             IDENTIF. ERROR
             HEADER READ  XXXX
             HEADER 07
             HEAD-
             EXPECTED = FF (FF = DATA)
             HEAD  - SECTOR EXPECTED XXXX
                     (same $)

            -IDENTIF.ERROR
             SECTOR  XXXX
             HEAD  - SECTOR EXPECTED XXXX
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       ENSEA
             XXXX STUCK AT 0 OR 1
             XXXX = faulty signal on output of ENSEA gate (CSE00 -CSE07)

            -STATUS PORT TO IDENTIF. XXXX
             HEAD  - SECTOR EXPECTED XXXX
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       RIERA
             XXXX STUCK AT 0 OR 1
             XXXX = faulty signal on output of RIERA gate (ERP01, ERDA1,
                    ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

            -SIGNAL PORT PRINO=INTERRUPT XXXX
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       FLAGA
              XXXX STUCK AT 0 OR 1
              XXXX = faulty signal on output of FLAGA gate (FOLTO,
                     ERBUI, PAERO, RESEB, PRINO)

            -IDENTIF.ERROR SELECT WITH HEADER 07
             IDENTIF.MUST BE FFFFFFFF

TEST 19:    -CYL - SIGN.WRITTEN ON SECTOR
           * CHECK BYTE DATA SECTOR
(3)        * FOUND ERROR ON BYTE N. XXXX
         $$ * CRT.EXPECTED XXXX
            * CRT.FOUND    XXXX
            * ADDRESS RAM DEPOSIT DATA READ 20   XXXX

             -CYL + SIGNIF. WRITTEN ON SECTOR
                   (same $$)
```

```
                -DATA WRITTEN FROM BYTE 8 TO 256
                      (same $$)

                -BYTE SUBSEQUENT TO 256 OF SECTOR
                      (same $$)

                -N. OF SECTOR WRITTEN ON DRIVE
                      (same $$)

                -VALUE 0000
                      (same $$)

                -NO DATA FROM DRIVE TO RAM BOARD
                      (same $$)

TEST 20:        -IDENTIF.ERROR
                 FLAG CHECK
 (3)           * READ SECTORS WWWW
               * READ YYYY
               *  N. BYTE-SECT.FINAL ZZZZ
          $$$  *  OLIBUS SIGNAL READ BY INPUT INSTR.
               *              EITRA
               *  XXXX STUCK AT 0 OR 1
               *  XXXX = faulty signal on output of EITRA gate (DAC00 -DAC07)

                -IDENTIF.ERROR
                 CYL. + SIGNIF.
                       (same $$$)

                -IDENTIF.ERROR
                 CYL. - SIGNIF.
                       (same $$$)

                -IDENTIF.ERROR
                 HEADER READ
                       (same $$$)

                -IDENTIF.ERROR
                 SECTOR
                 READ SECTORS WWWW
                 READ YYYY
                 N. BYTE-SECT.FINAL ZZZZ
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                            ENSEA
                 XXXX STUCK AT 0 OR 1
                 XXXX = faulty signal on output of ENSEA gate (CSE00 -CSE07)
```

```
            -STATUS PORT TO IDENTIF. XXXX
             READ SECTORS WWWW
             READ YYYY
             N. BYTE-SECT.FINAL ZZZZ
             OLIBUS SIGNAL READ BY INPUT INSTR.
                      RIERA
             XXXX STUCK AT 0 OR 1
             XXXX = faulty signal on output of RIERA gate (ERP01,ERDA1,
                    ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

            -SIGNAL PORT PRINO=INTERRUPT XXXX
             READ SECTORS WWWW
             READ YYYY
             N. BYTE-SECT.FINAL ZZZZ
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       FLAGA
              XXXX STUCK AT 0 OR 1
              XXXX = faulty signal on output of FLAGA gate (FOLT0,
                     ERBUI, PAERO, RESEB, PRINO)


TEST 21:     -IDENTIF.ERROR
              FLAG CHECK XXXX)
            * SECTOR READ =00 EXPECTED =01 XXXX
            * OLIBUS SIGNAL READ BY INPUT INSTR.
      $$$$ *          EITRA
            * XXXX STUCK AT 0 OR 1
            * XXXX = faulty signal on output of EITRA gate (DAC00 -DAC07)

             -IDENTIF.ERROR
              CYL. + SIGNIF. XXXX
                     (same $$$$)

             -IDENTIF.ERROR
              CYL. - SIGNIF. XXXX
                     (same $$$$)

             -IDENTIF.ERROR
             -HEADER READ  XXXX
                    (same $$$$)

             -IDENTIF.ERROR
             -SECTOR  XXXX
                    (same $$$$)

             -IDENTIF.ERROR
              SECTOR
              SECTOR READ =00 EXPECTED =01 XXXX
              OLIBUS SIGNAL READ BY INPUT INSTR.
                        ENSEA
              XXXX STUCK AT 0 OR 1
              XXXX = faulty signal on output of ENSEA gate (CSE00 -CSE07)
```

```
                -STATUS PORT TO IDENTIF. XXXX
                 SECTOR READ =00 EXPECTED =01 XXXX
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                        RIERA
                 XXXX STUCK AT 0 OR 1
                 XXXX = faulty signal on output of RIERA gate (ERPO1,ERDA1,
                        ERCE1, ERSY1, ERTI1, ERAN1, ERWO1, FIERA)

                -SIGNAL PORT PRINO=INTERRUPT XXXX
                 SECTOR READ =00 EXPECTED =01 XXXX
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                        FLAGA
                  XXXX STUCK AT 0 OR 1
                  XXXX = faulty signal on output of FLAGA gate (FOLTO,
                         ERBU1, PAERO, RESE8, PRINO)

TEST 22:        -VERIFY WITH CORRECT POSIT.
                 SECTOR READ AND VERIFIED = XXXX
                * OLIBUS SIGNAL READ BY INPUT INSTR.
                *        RIERA
     $$$$$      * XXXX STUCK AT 0 OR 1
                * XXXX = faulty signal on output of RIERA gate (ERPO1,ERDA1,
                *        ERCE1, ERSY1, ERTI1, ERAN1, ERWO1, FIERA)

                -DMARO=0 FOR ERCE-ERDA=1
                 SECTOR READ AND VERIFIED = XXXX
                       (same $$$$$)

                -TIOP0=0 FOR ERDA=1
                 SECTOR READ AND VERIFIED = XXXX
                       (same $$$$$)

                -TIOP3=1 FOR ERDA=1
                 SECTOR READ AND VERIFIED = XXXX
                       (same $$$$$)

                -TIP23=1 FOR ERDA=1
                 SECTOR READ AND VERIFIED = XXXX
                       (same $$$$$)

                -TIOP3=1 TIP12-DMARO=0 FOR ERDA=1
                 SECTOR READ AND VERIFIED = XXXX
                       (same $$$$$)

                -TIOP3-TIP12-DMARO=0 FOR ERDA=1
                 SECTOR READ AND VERIFIED = XXXX
                       (same $$$$$)
```

```
            -EXPECTED PRINO-RESEB=1 FOLTO =0
             SECTOR READ AND VERIFIED = XXXX
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       FLAGA
              XXXX STUCK AT 0 OR 1
              XXXX = faulty signal on output of FLAGA gate (FOLTO,
                     ERBUI, PAERO, RESEB, PRINO)

TEST 23:    -FIRST BYTE WITH A WRONG BIT
             * VALUE WRITT.IN SECTOR = XXXX
 (3)         * VALUE WITH DIFFERENT BIT= YYYY
             * STATUS RIERA FOR WRONG TEST
             * OLIBUS SIGNAL READ BY INPUT INSTR.
           & *                 RIERA
             * XXXX STUCK AT 0 OR 1
             * XXXX = faulty signal on output of RIERA gate (ERPO1,ERDA1,
             *          ERCE1, ERSY1, ERTI1, ERAN1, ERWO1, FIERA)

            -255TH BYTE WITH A WRONG BIT
                    (same &)

            -EXPECTED PRINO
             VALUE WRITT.IN SECTOR = XXXX
             VALUE WITH DIFFERENT BIT= YYYY
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       FLAGA
              XXXX STUCK AT 0 OR 1
              XXXX = faulty signal on output of FLAGA gate (FOLTO,
                     ERBUI, PAERO, RESEB, PRINO)

            -OUTPUT BURST NOT VALID BECOO=0
             VALUE WRITT.IN SECTOR = XXXX
             VALUE WITH DIFFERENT BIT= YYYY
             OLIBUS SIGNAL READ BY INPUT INSTR.
                       INBEP
              XXXX STUCK AT 0 OR 1
              XXXX = faulty signal on output of INBEP gate (PAMA2 - PAMA4,
                     AEBEO, EPBEO, BECOO, ROUT1, ROUT2)

TEST 24:  * -SELECT. POSHO
          *  TO ERROR BURST AMZ8065
 (3)      *  VALUE WRITT.IN SECTOR = XXXX
       && *  VALUE WITH DIFFERENT BITS = YYYY
          *  WORD NUMBER(256BYTE)   = ZZZZ
          *  CLOBE CLOCK NUMBER EXPECT.= VVVV
          *  CLOBE CLOCK NUMBER SENT
             EMISS. N. > CLOBE CLOCK

            -        (same &&)
             EMISS. N. < CLOBE CLOCK
```

```
                -       (same &&)
                 BUS INPUT RESLA NOT CORRECT
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          RESLA
                  XXXX STUCK AT 0 OR 1
                  XXXX = faulty signal on output of RESLA gate (L0EP0 - L0EP3,
                         RESK1 -RESK4)

                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          RESHA
                  XXXX STUCK AT 0 OR 1
                  XXXX = faulty signal on output of RESHA gate (B0U00 - B0U70)

                -       (same &&)
                 BUS INPUT RESHA NOT CORRECT
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          RESLA
                  XXXX STUCK AT 0 OR 1
                  XXXX = faulty signal on output of RESLA gate (L0EP0 - L0EP3,
                         RESK1 -RESK4)
                 OLIBUS SIGNAL READ BY INPUT INSTR.
                          RESHA
                  XXXX STUCK AT 0 OR 1
                  XXXX = faulty signal on output of RESHA gate (B0U00 - B0U70)

                -       (same &&)
                 MAX CLOCK N.,CORRECT. BIT.NOT=1

                -SELECT. POSH1
                        (same POSH0 above)

                -SELECT. POSH2
                        (same POSH0 above)

                -SELECT. POSH3
                        (same POSH0 above)

TEST 25:        -SIGNAL LUINO=1 PRINO=0
                * SECTOR WRITTEN = XXXX
  (3)           * OLIBUS SIGNAL READ BY INPUT INSTR.
                *          FLAGA
       &&&      *  XXXX STUCK AT 0 OR 1
                *  XXXX = faulty signal on output of FLAGA gate (FOLTO,
                *         ERBUI, PAERO, RESEB, PRINO)

                -SIGNAL LUINO=0 PRINO=1
                 SECTOR WRITTEN = XXXX (XXXX = DATA)
                          (same &&&)
```

```
-TO REGISTR.ON CYL.024A
 SECTOR WRITTEN = XXXX (XXXX = DATA)
 OLIBUS SIGNAL READ BY INPUT INSTR.
              RIERA
 XXXX STUCK AT 0 OR 1
 XXXX = faulty signal on output of RIERA gate (ERP01,ERDA1,
        ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

-TRANSFER. > 256 BYTES
 SECTOR WRITTEN = XXXX
 DATA WRITTEN ON DRIVE = YYYY
 DATA FOUND AFTER WRITE = ZZZZ
 NUMBER OF WRONG BYTES = WWWW

TEST 26:

-FORMAT.CYL.024A-NOT PRINO=1
 HEADER & SECTOR USED = XXXX
 OLIBUS SIGNAL READ BY INPUT INSTR.
              FLAGA
  XXXX STUCK AT 0 OR 1
  XXXX = faulty signal on output of FLAGA gate (FOLTO,
         ERBUI, PAERO, RESEB, PRINO)

-FORMAT.CYL.024A-WRONG END
 HEADER & SECTOR USED = XXXX
 OLIBUS SIGNAL READ BY INPUT INSTR.
              RIERA
 XXXX STUCK AT 0 OR 1
 XXXX = faulty signal on output of RIERA gate (ERP01,ERDA1,
        ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

-1 WRONG IDENTIF. / <= 9 BIT
 HEADER & SECTOR USED = XXXX
 VALUE IN REG.FILE (EILCA) EXPECT. = XXXX
 VALUE IN REG. FILE (EILCA) FOUND = XXXX
 16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX

-2 WRONG IDENTIF. /  > 9 BIT
 HEADER & SECTOR USED = XXXX
 VALUE IN REG.FILE (EILCA) EXPECT. = XXXX
 VALUE IN REG. FILE (EILCA) FOUND = XXXX
 16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX

-READ SECTOR AFTER ERROR = ERW01
 HEADER & SECTOR USED = XXXX
 DATA AREA WRITT.FOR DEFAULT= 0000 XXXX
 DATA AREA READ AFTER FORMATT= XXXX
 N. OF WRONG BYTES IN TEST = XXXX
```

```
          -READ SECTOR AFTER ERROR = ERTI1
           HEADER & SECTOR USED = XXXX
           DATA AREA WRITT.FOR DEFAULT= 0000 XXXX
           DATA AREA READ AFTER FORMATT= XXXX
           N. OF WRONG BYTES IN TEST = XXXX

          -ERROR STATUS EXPECTED IN WRITE= 40
           HEADER & SECTOR USED = XXXX
           16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX
         * OLIBUS SIGNAL READ BY INPUT INSTR.
         *              RIERA
&&&& *    XXXX STUCK AT 0 OR 1
         *  XXXX = faulty signal on output of RIERA gate (ERP01,ERDA1,
         *         ERCE1, ERSY1, ERTI1, ERAN1, ERW01, FIERA)

          -STATUS ERROR EXPECTED IN WRITE= 10
           HEADER & SECTOR USED = XXXX
           16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX
                     (same &&&&)

          -STATUS ERROR EXPECTED IN READ= 40
           HEADER & SECTOR USED = XXXX
           16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX
                     (same &&&&)

          -STATUS ERROR EXPECTED IN READ= 10
           HEADER & SECTOR USED = XXXX
           16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX
                     (same &&&&)

           PHYSICAL READ AFTER FORMAT= IDENTIF
           16 BYTE IDENTIF.WRITTEN FORMATT.TEST XXXX
           16 BYTE IDENTIF.READ AFTER FORMATT XXXX

          -AFTER FORMAT.DATA VALUE NOT 0000
           HEADER & SECTOR USED = XXXX
           DATA AREA WRITT.FOR DEFAULT= 0000 XXXX
           DATA AREA READ AFTER FORMATT= XXXX
           N. OF WRONG BYTES IN TEST = XXXX

          -PHYSICAL READ:TRANSFER.> 298 BYTE
           HEADER & SECTOR USED = XXXX
           DATA AREA WRITT.FOR DEFAULT = 0000 XXXX
           DATA AREA READ AFTER FORMATT= XXXX
           N. OF WRONG BYTES IN TEST = XXXX
```

15.6 F60TM3: FUJITSU (XU 1700)/SMD3 ROTATION TIME MEASUREMENT TEST

PROGRAM PURPOSE

To calculate the rotation and positioning time of the HDU.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (XU 1700, 60 Mbytes, single/dual ports), SMD3 adaptor and controller.

LOADING PROCEDURES

Refer to section 1.3.2.

15.6.1 TEST DESCRIPTION

TEST 1

This test calculates the HDU rotation time by initiating a read on a non existing sector which causes an interrupt to be generated and the system timer to be triggered. Then a further five reads are made and, on the last interrupt, the timer is stopped. The time measured between the first and last interrupt is the time taken for 10 revolutions of the HDU and is used to calculate the rotation time to an accuracy of 0.1%. When the time measured is greater than 1% of the average rotation time, an error message is displayed.

TEST 2

This test checks the positioning time of the HDU by using the system timer to determine the time taken to move track to track (5ms max) and 588 tracks (40ms max) in both the forward and reverse direction.

An error message is displayed at the end of the test if the maximum time is exceeded.

TEST 3

This test checks the positioning time of the HDU by using the system timer to measure the time taken to make successive seeks in steps defined by the operator from a lower cylinder to a higher cylinder and to return to the original cylinder. The test can be carried out on the whole disk or only on a section of the disk defined by the operator. bp **TEST 4**

This test determines the positioning time of the 60 MB FUJITSU peripheral unit.

The operator enters the value of the lower cylinder and the higher cylinder used by the program to calculate and display the positioning time (SEEK) and return time.

If the lower cylinder is 0, the SEEK return is a "HOME" operation.
Should the lower and higher cylinder be the same, the SEEK (or HOME) operation is not made and the message "TIME TOO SMALL TO BE MEASURED" is

displayed.

15.6.2 ERROR AND SERVICE MESSAGES

TYPE OF ERRORS INDICATED:
- TYPE A = errors recoverable using the program
- TYPE B = errors recoverable with the intervention of the operator
- TYPE C = hardware errors which are not recoverable on the PU or disk
- TYPE D = hardware errors which are not recoverable on the controller

TYPE B ERRORS

- UP NOT AVAILABLE
- UP BUSY
- UP NOT RECOGNISED

TYPE C ERRORS

- ERROR ON VERIFY
- ERROR ON IDENTIFIER
- ERROR ON READ COMMAND

TYPE C OR D ERRORS

- HARDWARE FAULT
- PERMANENT FAULT
- TEMPORARY FAULT
- TIME OUT ERROR MEMORY ACCESS
- MEMORY ERROR
- SYITEM BUS ERROR
- INCOHERENT ANSWER

15.7 SM12V4: FUJITSU (XU1700)/SMD3 VERIFY AND CORRECTION PROGRAM

PROGRAM PURPOSE

To display the contents of the HDU data field and condition of disk (no. of faulty tracks, alternative tracks etc.), verify and certify tracks and sectors, and also assign and format alternative tracks.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (XU 1700/M2312K, 60 Mbytes, single/dual ports), SMD3 adaptor and controller.

NOTE:

Data is destroyed when certifying or formatting using this program. A dump operation must be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES

Refer to section 1.3.2.

15.7.1 TEST DESCRIPTION

1. Verifies a track with a series of data field reads.

2. Verifies a sector with a series of reads.

3. Certifies a track by performing a series of write and read operations using a default pattern or a pattern entered by the operator.

4. Certifies a sector by performing a series of write and read operations using a default pattern or a pattern entered by the operator.

5. Displays the data field of one or more sectors in HEX. and ISO characters.

6. Display a MENU from which three operations may be performed:

   a) Check identifier:

   b) Formatting track:

   c) Search first free alternative track:

7. Displays the disk condition, track per track, with the exception of the test track.

15.7.2 ERROR MESSAGES

TYPE OF ERRORS INDICATED:
- TYPE A = errors recoverable using the program
- TYPE B = errors recoverable with the intervention of the operator
- TYPE C = hardware errors which are not recoverable on the PU or disk
- TYPE D = hardware errors which are not recoverable on the controller

TYPE B ERRORS

- PU BUSY
- PU NOT READY
- PU IN WRITE PROTECT CONDITION
- UNKNOWN PU
- ABSENT PU
- TOO MANY PU SELECTED!!
- CONTROLLER AND ADAPTER BUSY
- CONTROLLER ABSENT
- UNKNOWN CONTROLLER

TYPE C OR D ERRORS

- TIME-OUT ERROR
- HARDWARE ERROR
- INCOHERENT REPLY

TYPE C ERRORS

- ERROR DURING READ PHASE
- ERROR DURING WRITE PHASE
- TEMPORARY DRIVE FAILURE
- PERMANENT DRIVE FAILURE

TYPE D ERRORS

- CONTROLLER NOT RESET
- SYSTEM BUS ERROR

16.1 2322F5: FUJITSU/SMD3 (XU1703) DISK FORMATTER PROGRAM

PROGRAM PURPOSE

To format the FUJITSU/SMD3 hard disk unit when connected to a SMD3 sub-system.

REQUIRED HARDWARE

FUJITSU/SMD3 hard disk unit (M2322K, 120 Mbytes, single/dual ports), host adaptor SMD3 and controller.

PRELIMINARY WARNING

The disk must be certified by the manufacturer (FUJITSU) and have at least one ermap otherwise formatting is carried out without assigning alternative tracks or initializing the data field.

Also note that any data on the disk before formatting is lost.

Formatting time : approx. 1/2 Hour.

LOADING PROCEDURE

Refer to section 1.3.2.

16.1.1 TEST DESCRIPTION

Refer to the TEST DESCRIPTION for the SM23F6 program (section 15.1.1).

16.1.2 ERROR MESSAGES

Refer to the ERROR MESSAGES for the SM23F6 program (section 15.1.2).

16.2 120ST1: WRITE STANDARD 24 ON FUJITSU/SMD3 (XU1703)

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 and 12 of track 0, cylinder 0.

HARDWARE REQUIRED

FUJITSU/SMD3 disk unit (M2322K, 120 Mbytes, dual/single port), host adapter SMD3 and controller.

LOADING PROCEDURE

Refer to section 1.3.2.

16.2.1 TEST DESCRIPTION

The adaptor and controller are initialized and then the data defined by STANDARD 24 is written on sectors 7, 8, and 9 of track 0, cylinder 0 and repeated again on the same track on sectors 10, 11, and 12.

16.2.2 ERROR MESSAGES

Refer to the ERROR MESSAGES for the SM23F6 program (section 15.1.2).

16.3 2322E3: FUJITSU/SMD3 (XU1703) ERROR RATE PROGRAM

PROGRAM PURPOSE

To check the reading and writing operation of a FUJITSU/SMD3 disk unit when connected to a SMD3 subsystem and operating under normal user mode.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (M2322K, 120 Mbytes, single/ dual port), host adaptor SMD3 and controller.

OPERATING PROCEDURE

Refer to introduction section in chapter 1

PRELIMINARY WARNING

The write operation in this program destroys data present on the disk. A dump operation should be made before commencing tests if data is to be preserved.

16.3.1 TEST DESCRIPTION

Refer to the TEST DESCRIPTION for the 2312E8 program (section 15.3.1).

16.3.2 ERROR MESSAGES

Refer to the ERROR MESSAGES of the 2312E8 program (section 15.3.2).

16.4 FJSCT3: FUJITSU (XU1703)/SMD3 and STC SAVE-RESTORE PROGRAM

PROGRAM PURPOSE

To evaluate the error rate of the FUJITSU/SMD3 subsystems and the STC subsystem by writing and reading sample patterns under critical conditions and performing SAVE (disk to tape) and RESTORE (tape to disk) operations.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (XU1703/M2322K, 120 Mbytes, single/dual ports), SMD3 adaptor and controller, streaming tape cartridge unit (STC), STC adaptor and controller.

PRELIMINARY WARNING

The write, save and restore operations in this program destroys data present on both disk and tape units. A dump operation on each unit should be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES

Refer to section 1.3.2.

16.4.1 TEST DESCRIPTION

Refer to the TEST DESCRIPTION of the 23SCT3 program (section 15.4.1).

16.4.2 ERROR MESSAGES

Refer to the ERROR MESSAGES of the 23SCT3 program (section 15.4.2).

16.5 SM1211: SMD CONTROLLER (FOR XU1703) DIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To test the SMD3 adaptor and controller when connected to 1, 2, 3 or 4 FUJITSU/SMD3 hard disk units.

REQUIRED HARDWARE

FUJITSU/SMD3 hard disk unit (M2322K/XU1703, 823 cylinder, 120 Mbytes, single/dual ports), SMD3 adaptor and controller.

WARNING

The disk units connected to the SMD3 adaptor, which are not included in the test, may be left connected and ON LINE but must not be selected for the READ/WRITE test.

Cylinder 821 is reserved for the diagnostic tests. The cylinder must be formatted and must contain an OLIVETTI test program.

Cylinder 820 track 06 must not contain any errors.

NOTE

The tests 1 to 26 must be carried out sequentially with the exception of tests 15 to 16 which may be omitted if the following conditions are prevelant:

-test 15 ; the RAM size is not known and the test gives an error,

-test 16 ; the reserved test cylinder is faulty.

LOADING PROCEDURES

Refer to section 1.3.2.

16.5.1 TEST DESCRIPTION

Refer to the TEST DESCRIPTION for the SM0611 program (section 15.5.1).

16.5.2 ERROR MESSAGES

Refer to the ERROR MESSAGES of the SM0611 program (section 15.5.2).

16.6 F12TM3: FUJITSU (XU 1703)/SMD3 ROTATION TIME TEST

PROGRAM PURPOSE

To calculate the rotation and positioning time of the HD unit.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (XU 1703, 120 Mbytes, single/dual ports), SMD3 adapter and controller.

LOADING PROCEDURES

Refer to section 1.3.2.

16.6.1 TEST DESCRIPTION

Refer to the TEST DESCRIPTION of the F60TM3 program (section 15.6.1).

16.6.2 SERVICE MESSAGES

Refer to the ERROR MESSAGES of the F60TM3 program (section 15.6.1).

16.7 SM22V2: FUJITSU (XU1703)/SMD3 VERIFY AND CORRECTION PROGRAM

PROGRAM PURPOSE

To display the contents of the HDU data field and condition of disk (no. of faulty tracks, alternative tracks etc.), verify and certify tracks and sectors, and also assign and format alternative tracks.

HARDWARE REQUIRED

FUJITSU/SMD3 hard disk unit (XU1703/M2322K, 120 Mbytes, single/dual ports), SMD3 adaptor and controller.

NOTE:

Data is destroyed when certifying or formatting using this program. A dump operation must be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES

Refer to section 1.3.2.

16.7.1 TEST DESCRIPTION

Refer to the TEST DESCRIPTION of the SM12V4 program (section 15.7.1).

16.7.2 ERROR MESSAGES

Refer to the ERROR MESSAGES of the SM12V4 program (section 15.7.2).

17.1 HDC5F5: XU 1707/1709 HARD DISK FORMATTER PROGRAM

PROGRAM PURPOSE

To format the hard disk unit(HDU) when connected to an HDC5 subsystem.

REQUIRED HARDWARE

CPU board, RAM board, XU 1707/1709 (WREN1/2) hard disk unit (27/65 MB, single port) and G0363 controller.

PRELIMINARY WARNING

This program can only be run on a disk which contains data defined by STANDARD 24 on track 0.

Also the disk must be certified by the manufacture and have at least one ermap otherwise formatting is carried out without assigning alternative tracks.

Note: any data on the disk before formatting is lost.

Formatting time : approx. 1/4 Hour.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.1.1 TEST DESCRIPTION

The program determines if the controller is in the correct slot position, identifies the peripheral unit to be formatted and then proceeds with the following operations in the order indicated:

1. STANDARD NO 24 READ PHASE...

   Reads the STANDARD 24 data on track 0 to determine the ETF, USER AREA and the DIAGNOSTIC AREAS as well as the other operating parameters.

   If this data is not present, the disk cannot be formatted and the program ends.

2. ETF READ PHASE...

   Reads the manufacturer's ermap (ETF). If the ETF cannot be read, the operator is requested if formatting is still required without assigning alternative tracks.

3. FORMAT PHASE...

   Formats the USER AREA (excluding the DIAGNOSTIC AREAS) assigning alternative tracks (if any) as indicated in the ETF.

4. VERIFY IDENTIFIER PHASE ...

   Checks the tracks just formatted to see if there are any SEEK errors by checking that there is at least one correct identifier on each track.

   3 attempts are made to recover errors.

5. WRITE & VERIFY DATA FIELD PHASE ...

   Writes the pattern %00 on the USER AREA (excluding the DIAGNOSTIC AREAS) and verifies the data written.

6. CERTIFY, FORMAT & WRITE
   OF DIAGNOSTIC AREAS ...

   Performs the following operations on all three types of track:

   a) WRITE TEST TRACKS:

      Writes a test pattern on each WRITE TEST TRACK followed by a read of the same track to see if there are any faulty sectors. This operation is repeated 200 times to certify the track. The program then sets the ERROR-FREE flag on the corresponding READ ONLY TEST TRACK according to results.

   b) READ ONLY TEST TRACKS:

      Formats all the READ ONLY TEST TRACKS in reduced mode. Test patterns are then written on the tracks, taking into account the contents of the sector containing the WRITE TRACK FLAGS. Each track is then read 200 times to see if there are any faulty sectors.

   c) DIAGNOSTIC SERVICE TRACKS:

      Formats all the DIAGNOSTIC SERVICE TRACKS in reduced mode. Then writes a test pattern on each track followed by a read to see if there are any faulty sectors. This operation is repeated 200 times.

If there are errors the faulty track is re-formatted in reduced mode.

At the end of tests a program summary is produced to indicate results, see section on ERROR AND SERVICE MESSAGES.

17.1.2 ERROR AND SERVICE MESSAGES

Before changing disk check the controller using the diagnostic test program.

a) **CONFIGURATION/INITIALISATION ERRORS**

- **PU ABSENT:**
  indicates that the peripheral selected is not connected to the controller.

- **PU NOT READY**
  WAIT ABOUT 2 MINUTES, PLEASE ...:
  re-load the program if error persists or if message appears during program execution the peripheral unit is considered faulty.

- **CONTROLLER INITIALISATION ERROR:**
  the program makes 3 attempts to correct the fault, if the error persists the peripheral unit is considered faulty.

b) **SUPPORT DATA ERRORS**

- **TRACK 0 UNREADABLE! TRY TO INSTALL STD24**
  PROGRAM ABORTS:
  informs the operator that track 0 is unreadable; the disk should be re-certified using the appropriate WRITE STANDARD 24 program.

- **STD 24 RECORDED ON TRACK 0 NOT CORRECT! TRY TO INSTALL STD24**
  PROGRAM ABORTS:
  informs the operator that data contained on track 0 does not correspond with conditions found on disk; track 0 should be re-certified using the appropriate WRITE STANDARD 24 program.

- **ETF NOT READABLE**
  DO YOU WANT TO FORMAT WITHOUT USING ETF? (YES = 451, NO = ANY KEY):
  informs the operator that the manufacturer's ermap is not readable and requests if formatting is required without assigning alternative tracks.

c) **POSITIONING ERRORS**

- **HOME ERROR:**
  this error results when a HOME command is not effected; 5 HOME operations are attempted before the program is aborted.

- **SEEK ERROR:**
  CYL: XXX HD: XX :
  this error results when a SEEK command is not effected; 5 SEEK operations are attempted with a HOME operation between each attempt before the program is aborted.

- **LANDING ZONE POSITIONING ERROR:**

  this error results when the HEAD is not correctly positioned on the LANDING ZONE at the end of the program.

d) **FORMATTING ERRORS**
After formatting the program tests the identifiers of the tracks just formatted. If errors are found, 5 attempts are made to format the tracks. A HOME operation is performed before each attempt. If the errors are not cleared the following messages may be displayed:

- **ERROR IN VERIFY FORMATTING PHASE**
  CYL: XXX HD: XX :
  indicates errors found (on cylinder: XXX, head XX) during the formatting phase; the program then continues with the remaining tests.

- **NON FORMATTED TRACK DETECTED**
  VERIFY FORMAT PHASE! PROGRAM ABORTS:
  indicates that a track has been found without any identifiers during the recovery attempts; the program then aborts.

e) **REGISTRATION/CERTIFICATION ERRORS**

- **DEFECTIVE TRACK**
  CYL: XXX HD: XX :
  displayed if during registration a track has been found containing a number of defective sectors; the defective cylinder(s) XXX and head(s) XX are listed and then the program continues with the remaining tests.

- **DISK UNRELIABLE !**
  PROGRAM ABORTS
  displayed if a track has been found containing a number of defective sectors greater than or equal to the acceptable "maximum number of bad sectors per track"; the program then aborts.

f) **HARDWARE ERRORS**
One attempt is made to correct the following errors before the error message is displayed and the program aborted.

- **INCOHERENT CONTROLLER RESPONSE**
  HARDWARE ERROR:
  indicates the result of an I/O routine which is not as expected in the program.

- **HARDWARE FAILURE**
  TIME OUT DURING I/O OPERATION

- **HARDWARE FAILURE**

- **HARDWARE FAILURE**
  PU ERROR
  indicates peripheral unit failure

g) **SUMMARY SERVICE MESSAGES**
The following messages are displayed at the end of the program:

- **PROGRAM EXECUTED WITHOUT**
  USING ETF INFORMATION:
  displayed if the ermap is illegible or not present and the operator has decided to run the program anyway.

- **DISK CORRECTLY FORMATTED:**
  displayed if disk is correctly formatted and contains only the errors listed in the EFT.

- **THE DISK IS RECOVERABLE BUT IS CRITICAL**
  DO NOT RESTART PROGRAM, USE SPECIFIC
  DIAGNOSTIC PROGRAM TO VERIFY THE
  FOLLOWING TRACK(S):
  CYL: XXX HD: XX
  CYL: XXX HD: XX
  : : :
  : : :
  CYL: XXX HD: XX
  displayed if the disk has been correctly formatted but contains errors on the identifier field or data field which are not present on the ETF.; the defective cylinder(s) XXX and head(s) XX are listed as shown.

- **DISK NOT FORMATTED BECAUSE THERE ARE**
  TOO MANY BAD SECTORS ON A GIVEN TRACK
  displayed if more defective sectors than the acceptable "maximum number of bad sectors per track" has been found on a READ ONLY TEST TRACK, a WRITE TEST TRACK or a DIAGNOSTIC SERVICE TRACK; the defective cylinder(s) XXX and head(s) XX are listed and the program is aborted.

- **HARDWARE FAILURE**
  DISK NOT FORMATTED
  displayed if there is a hardware failure.

- **PROGRAM CANNOT BE RUN ON THIS PU**
  diplayed if the support data (i.e. STANDARD 24 data on track 0) is incorrect or missing.

- **ETF NOT READABLE**
  DISK NOT FORMATTED
  displayed when the operator has decided not to format the disk following an ETF NOT READABLE message.

- **THERE ARE NO MORE ALTERNATIVE**
  TRACKS IN ORDER TO ASSIGN FAULTY TRACK
  displayed if the ETF indicates that all the alternative tracks have been used.

17.2 HDC5E7: XU 1707/1709 ERROR RATE PROGRAM

PROGRAM PURPOSE

To check the reading and writing operation of an XU1707/1709 hard disk unit when connected to a HDC5 subsystem and operating under normal user mode.

HARDWARE REQUIRED

CPU board, RAM board, XU1707/1709 (WREN1/2) hard disk unit (27/65 MB, single port) and G0363 controller.

PRELIMINARY WARNING

The write operation in this program destroys data present on the disk. A dump operation should be made before commmencing tests if data is to be preserved.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.2.1 TEST DESCRIPTION

WRITE & VERIFY FORWARD (FROM OUTERMOST TO INNERMOST CYLINDER) - TEST 1

Writes test pattern on a number of defined sectors and successively verifies the data written. The test is effected using incremental addressing.

Tests are limited to specific cylinders when cylinder step is NOT 1 and the ALL SURFACES parameter is NOT selected in the pre-program.

READ BACK (FROM INNERMOST TO OUTERMOST CYLINDER)- TEST 2

Reads the sectors defined in the initial part of the program and if COMPARE DATA is selected, compares the data read with the data in memory used in TEST 1/3. If COMPARE DATA is NOT selected, the data read is checked to see if it corresponds with the ECC value.

The test is carried out using decremental addressing.

WRITE & VERIFY BACK (FROM INNERMOST TO OUTERMOST CYLINDER)- TEST 3

The test is similar to TEST 1 except that data is written using decremental addressing.

READ FORWARD (FROM OUTERMOST TO INNERMOST CYLINDER)- TEST 4

The test is similar to TEST 2 except that data is read using incremental addressing.

READ RANDOM - TEST 5

The test is similar to TEST 2 except that data is read using random addressing and random transfer lengths (the transfer length entered in the pre-program is ignored). An algorithm is used to generate the cylinder and head ranges and the transfer lengths.

17.2.2 ERROR AND SERVICE MESSAGES

Use verify and correction program to re-allocate tracks where indicated.

In cases where the error message indicates that the disk is faulty (i.e. NOT recoverable) use the controller diagnostic test program to check the controller before replacing the disk.

a) **CONFIGURATION/INITIALISATION ERRORS**

Refer to the corresponding section (17.1.2) of the HDC5F5 program.

b) **POSITIONING ERRORS**

As listed in the corresponding section of the HDC5F5 program with the following addition displayed when a SEEK command fails:

- **WRONG CYLINDER SELECTED**
  EXPECTED CYL=XXX SELECTED CYL=YYY:

  displayed when the cylinder selected is recognised by the program but is NOT the expected cylinder.

- **UNKNOWN CYLINDER SELECTED**
  EXPECTED CYL=XXX:

  displayed when the cylinder selected is NOT recognised by the program.

- **WRONG HEAD SELECTED ON CYL=XXX:**
  EXPECTED HD=XXX SELECTED HD=YYY:

  displayed when the head selected is NOT the selection expected by the program.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO CYL= YYY:

  displayed when a cylinder positioning is lost and the program has stopped on cylinder YYY.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO UNKNOWN CYL:

  displayed when cylinder positioning is lost and the program is NOT able to determine on which cylinder the program has stopped.

- **SECTOR IDENTIFIER NOT FOUND**
  CYL=XXX HD=Y SECT=ZZZ:

  displayed once only when the identifier of a sector is NOT recognised or is illegible or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected (i.e. set to 1).

- **DATA FIELD NOT FOUND**
  CYL=XXX HD=Y SECT=ZZZ:

  indicates that the synchronisation characters preceding the data of a sector are NOT recognised; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected.

c) **WRITE ERRORS**

- **DATA FIELD WRITE ERROR**
  CYL: XXX HD: YY SECT: ZZZ

  indicates an error on a sector during a WRITE operation; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected.

- **ERROR ON CYL: XXX HD: YY SECT: ZZZ**
  WRITE NUMBER: UUUUUU
  DATA FIELD ERRORS N: VVVVVV
  DATA MARK NOT FOUND N: WWWWWW
  ERROR RATE: ID= > OR < xx% DATA= > OR < yy%
  MAX CONSECUTIVE ID OR DATA ERR: zzzzz:

  displayed if a WRITE operation on a sector fails; note that the result of the error rate calculations are given together with the address of the faulty sector and that any non-significant field is indicated with "?" (xx/yy= threshold value entered by the operator)

d) READ ERRORS

- RECOVERED DATA FIELD READ ERROR
  CYL: XXX HD: YY SECT: ZZZ
  BURST LENGTH: xxx
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy:

  indicates that a READ error on a sector is recovered by ECC; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected; note that the sector address, burst length, write pattern, read pattern and displacement characters (from the start of the sector to the first incorrect character) are indicated.

- UNRECOVERED DATA FIELD READ ERROR
  CYL: XXX HD: YY SECT: ZZZ
  BURST LENGTH: xxx
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy:

  indicates that a READ error on a sector is NOT recovered by ECC; displayed once only or each time the error occurs if the DISPLAY ERRORS EACH TIME parameter has been selected; note that the same parameters as above are indicated.

- ERROR ON CYL: XXX HD: YY SECT: ZZZ
  READ NUMBER: UUUUUU
  DATA FIELD ERRORS N: VVVVVV
  RECOVERABLE ERRORS: WWWWWW
  UNRECOVERABLE ERRORS: wwwwww
  ECC CORRECTION FAILURES: uuuuuu
  DATA MARK NOT FOUND: vvvvvvv
  BURST LENGTH
  MAX: mmm MIN: nnn
  SECTOR NOT FOUND N: aaaaaa
  ERROR RATE: ID= > OR < xx% DATA= > OR < yy%
  MAX CONSECUTIVE ID OR DATA ERR: zzzzz:

  displayed if a READ operation on a sector fails; note that the result of the error rate calculations are given together with the address of the faulty sector and other relevant parameters; any non-significant field is indicated with "?" (xx/yy= threshold value entered by the operator).

e) HARWARE ERRORS
The following messages are self explainatory and are displayed as the result of the hardware error counter threshold value being exceeded.

- INCOHERENT I/O CONTROLLER ANSWER
  HARDWARE ERROR

- MEMORY TRANSFER DATA NOT DETECTED
  BY THE SYSTEM. HARDWARE FAILURE
  CYL: XXX HD: YY SECT: ZZZ
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy

- HARDWARE GAVE WRONG INFORMATION ON
  EITHER BURST LENGTH OR BURST POSITION
  OF A RECOVERED DATA FIELD READ ERROR
  CYL: XXX HD: YY SECT: ZZZ
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy

- TIME OUT DURING I/O OPERATION
  HARDWARE FAILURE

- HARDWARE FAILURE

  indicates general hardware failure.

- PU HARDWARE FAILURE

  indicates peripheral unit (disk) hardware failure.

f) ECC NETWORK ERRORS

- ECC RECOVERALBE READ ERROR
  NOT REALLY RECOVERED!
  CYL: XXX HD: YY SECT: ZZZ
  BEFORE ECC CORRECTION:
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy
  AFTER ECC CORRECTION:
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy:

  indicates that the ECC has declared a read error recoverable but in fact has NOT been able to recover the error; the sample pattern and the data read before the correction are displayed together with the sample pattern and the data read after the attempted correction; the error is also indicated in the summary messages.

- **READ ERROR INCORRECTLY**
  DECLARED RECOVERABLE
  CYL: XXX HD: YY SECT: ZZZ
  BEFORE CORRECTION:
  REF. vvvvvvvvv
  TST. wwwwwwwww
  DISPLACEMENT CRT: yyyyy

  indicates that a read error has been declared recoverable when in fact the error burst is greater than the number of bits needed for the correction; the sample pattern and the data read before the attempted correction are displayed; the error is also indicated in the summary messages.

g) **SUPPORT DATA ERRORS**

- **TRACK 0 UNREADABLE! TRY TO INSTALL STD24**
  PROGRAM ABORTS:
  informs the operator that track 0 is unreadable; the disk should be re-certified using the appropriate WRITE STANDARD 24 program.

- **STD 24 RECORDED ON TRACK 0 NOT CORRECT! TRY TO INSTALL STD24**
  PROGRAM ABORTS:
  informs the operator that data contained on track 0 does not correspond with conditions found on disk; track 0 should be re-certified using the appropriate WRITE STANDARD 24 program.

- **CANNOT READ HISTORY TRACK**
  informs the operator, following a selection of a READ HISTORY TRACK operation, that the DIAGNOSTIC SERVICE TRACK is not readable and terminates the program.

- **CANNOT WRITE HISTORY TRACK**
  PROGRAM ABORTS
  informs the operator, following a selection of a WRITE HISTORY TRACK operation, that a WRITE operation on the DIAGNOSTIC SERVICE TRACK cannot be made and aborts the program.

- **THE DEFAULT PARAMETERS ARE**
  VALID FOR ANOTHER TYPE OF DISK
  PROGRAM ABORTS
  informs the operator, that the default parameters entered during the MONITOR preprogram are not compatible with the disk.

h) **SUMMARY MESSAGES**

The following summary message is displayed at the end of the program:

```
********** SUMMARY ************
DATA EXCHANGE (IN SECTORS): XXXXXXXX
FROM CPU TO PU        XXXX
FROM PU TO CPU        XXXX
FROM PU TO CONTROLLER XXXX
CRITICAL SECTORS IN TOLERANCE: XXXXX
SECTORS OUT OF TOLERANCE.....: XXXXX
SECTORS TO BE RE-ALLOCATED...: XXXXX
HARDWARE ERRORS: XXXXXX
     DIAGNOSTIC RESULT
    JJJJJJ.....JJJJJJJ
```

WHERE:
JJJJJ...JJ = RELIABLE SUBSYSTEM/ RECOVERABLE SUBSYSTEM/ UNRELIABLE SUBSYSTEM

- **DATA EXCHANGE (IN SECTORS): XXXXXXXX**

  indicates data exchanged by the program, between PU/CPU/CONTROLLER, in terms of sectors transfered.

- **CRITICAL SECTORS IN TOLERANCE: XXXXX**

  indicates the number of sectors containing errors which have a calculated error rate still within the threshold value entered by the operator.

- **SECTORS OUT OF TOLERANCE.....: XXXXX**

  indicates the number of sectors containing errors which have a calculated error rate outside the threshold value entered by the operator during the pre-program.

- **SECTORS TO BE RE-ALLOCATED....:XXXXX**

  indicates the total number of sectors to be re-allocated including:

  a) sectors with at least one "DATA MARK NOT FOUND" error.

  b) sectors which have NOT been corrected by the ECC.

  c) sectors in which a read error has occured with a burst length greater than the value specified in STANDARD 24.

- **HARDWARE ERRORS: XXXXXX**

  indicates the number of hardware errors found with a frequency greater than the threshold value set for the hardware errors.

17.3 HD5ST3: XU 1707/1709 and STC SAVE-RESTORE PROGRAM

PROGRAM PURPOSE

To evaluate the error rate of the HDC5 subsystem and the STC subsystem by writing and reading sample patterns under critical conditions and performing SAVE (disk to tape) and RESTORE (tape to disk) operations.

HARDWARE REQUIRED

CPU board, RAM board, XU 1707/1709 (WREN1/2) hard disk unit (27/65 MB, single port) with G0363 controller, XU1120/1130 streaming tape cartridge unit (STC), G0201B/G0352 formatter and G0200 controller.

PRELIMINARY WARNING

The write, save and restore operations in this program destroys data present on both disk and tape units. A dump operation on each unit should be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

OPERATING PROCEDURES

Refer to section 1.3.2.

17.3.1 TEST DESCRIPTION

GENERAL

There are 10 tests/operations which can be selected by the operator.

1) WRITE HDU

Writes a test pattern which increments from %0000 to %7FFF on the HDU.

2) READ HDU

Reads the HDU and then compares in memory the data read with the original data used for writing. For the test to be valid operations must be made in the following order: erase tape, write on tape, restore data from tape to HDU and then read HDU.

3) WRITE TAPE

Writes a test pattern which decrements from %FFFF to %8000 on the tape. A write operation must always follow a tape erase operation.

4) READ TAPE

Reads the tape and then compared in memory the data read with the data originally used for writing on the disk. Operations must be made in the following order: erase tape, write on HDU, save data from HDU to tape and finally read tape.

5) HDU --> TAPE

The test comprises a save operation in which data is transfered from HDU to tape in overlapped mode (after each transfer the data is verified). Before each transfer the memory is erased by a cancellation pattern %AAAA.

6) TAPE --> HDU

The test comprises a restore operation in which data is transfered from the tape to the HDU in overlapped mode. Before each transfer the memory is erased by a cancellation pattern %5555.

7) PRECOND TAPE

The operation permits the tape to be pretentioned.

8) REWIND TAPE

The rewind operations are carried out automatically by the program but can be introduced in the test sequence if required.

9) ERASE TAPE

The erase operation MUST be introduced in the test sequence before a WRITE TAPE operation.

10) PAUSE

The pause operation can be introduced in the test sequence if require (to cool the tape unit).

17.3.2 ERROR AND SERVICE MESSAGES

Before replacing the disk or tape check the corresponding controller.

A) HDU MESSAGES:

a) CONFIGURATION/INITIALISATION ERRORS

- **PU ABSENT OR DOES NOT ACKNOWLEDGE:**
  indicates that the HDU selected is not connected to the controller or is not the correct unit.

- **PU NOT READY**
  re-load the program if error persists or if the message appears during program execution the HDU is considered faulty.

- **CONTROLLER INITIALISATION ERROR:**
  displayed if an error occurs during the initialisation phase of the controller.

b) SUPPORT DATA ERRORS

- **STANDARD 24 NOT FOUND**
  informs the operator that sector 15 of track 0 is unreadable; the disk should be re-certified using the appropriate WRITE STANDARD 24 program.

c) POSITIONING ERRORS

- **HOME ERROR:**
  this error results when a HOME command is not effected

- **SEEK ERROR:**

  this error results when a SEEK command is not effected

- **LANDING ZONE POSITIONING ERROR:**

  this error results when the HEAD is not correctly positioned on the LANDING ZONE at the end of the program.

- **WRONG CYLINDER SELECTED**
  EXPECTED CYL=XXX SELECTED CYL=YYY:

  displayed when the cylinder selected is recognised by the program but is NOT the expected cylinder.

- **UNKNOWN CYLINDER SELECTED**
  EXPECTED CYL=XXX:

  displayed when the cylinder selected is NOT recognised by the program.

- **WRONG HEAD SELECTED ON CYL=XXX:**
  EXPECTED HD=XXX SELECTED HD=YYY:

  displayed when the head selected is NOT the selection expected by the program.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO CYL= YYY:

  displayed when a cylinder positioning is lost and the program has stopped on cylinder YYY.

- **CYL POSITION LOST DURING I/O OPERATION**
  FROM CYL=XXX TO UNKNOWN CYL:

  displayed when cylinder positioning is lost and the program is NOT able to determine on which cylinder the program has stopped.

- **SECTOR IDENTIFIER NOT FOUND**
  CYL=XXX HD=Y SECT=ZZZ:

  displayed when the identifier of a sector is NOT recognised or is illegible.

- **DATA FIELD NOT FOUND**
  CYL=XXX HD=Y SECT=ZZZ:

  indicates that the synchronisation characters preceding the data of a sector are NOT recognised.

d) **HARDWARE ERRORS**

One attempt is made to correct the following errors before the error message is displayed and the program aborted.

- **INCOHERENT CONTROLLER ANSWER**
  HARDWARE ERROR:

  indicates the result of an I/O routine which is not as expected in the program.

- **HARDWARE FAILURE**
  TIME OUT DURING I/O OPERATION

- **HARDWARE FAILURE**

- **HARDWARE FAILURE**
  PU HARDWARE ERROR

  indicates peripheral unit failure
  ECC ERROR
  CYL=XXX HD=XX SECT=XX

  this message appears whenever the ECC finds an error regardless whether the error is recoverable or not.

B) STC MESSAGES Check the tape and controller before replacing the STC.

The STC messages are self-explanatory and are listed below:

- CARTRIDGE NOT INSERTED
- PERMISSION DENIED
  TAPE IN WRITE PROTECT MODE
- INTERRUPTION BY OPERATOR
- STC NOT READY
- CONTROLLER BUSY
- CONTROLLER INITIALISATION ERROR
- ERROR DURING WRITE: CARTRIDGE CRASH
- UNEXPECTED EOT (end of tape)
- WRITE ATTEMPTED ON TRACK NOT ERASED
- ONE BUFFER NOT TRANSFERED
- INCOHERENT CONTROLLER ANSWER
  HARDWARE ERROR
- TIME OUT DURING I/O OPERATION
  HARDWARE FAILURE

C) COMPARISON ERRORS

These messages are produced as the result of comparison tests between the data transfered and the original data before the transfer:

- ALL DATA NOT TRANSFERED
- SOME DATA NOT TRANSFERED
- WRONG DATA TRANSFERED
- WRONG BLOCK LABEL FOUND
  indicates that the sector or block identifiers found are NOT as expected.

These error messages are preceded with the following:

MEMORY TRANSFER ERROR NOT DETECTED
BY THE SYSTEM. HARDWARE FAILURE

D) SUMMARY SERVICE MESSAGES

The following messages are displayed at the end of the program:

1)
```
***** DIAGNOSTIC RESULT *******
PROGRAM COMPLETED/PROGRAM ABORT
```

NOTE:
The summary table of errors are ONLY displayed if the TEST is EXECUTED.

2)

```
 --TAPE TRANSFER SUMMARY--
 ============================
|READ BLOCKS:              |XXXXX|
|OPERATION(S) WITH REPET.:|    X|
|REPEATED BLOCK(S)        |    X|
 ----------------------------
|WRITTEN BLOCKS:           |XXXXX|
|OPERATION(S  WITH REPET.:|    X|
|REPEATED BLOCK(S)        |    X|
 ----------------------------
|COMPARE ERROR(S) :        |    X|
 ============================
```

3)

```
    ---HDU TRANSFER SUMMARY---
 ============================
|READ SECTORS:             |XXXXX|
|ERROR(S) DETECTED:        |    X|
 ----------------------------
|WRITTEN SECTOR            |XXXXX|
|ERROR(S) DETECTED:        |    X|
 ----------------------------
|COMPARE ERROR(S) :        |    X|
 ============================
```

17.4 HDC5V6: XU1707/1709 VERIFY AND CORRECTION PROGRAM

PROGRAM PURPOSE

To display the contents of the HDU data field and condition of disk (contents of factory ERMAP, list of alternative tracks used etc.), verify and certify tracks and sectors, and also assign and format alternative tracks.

HARDWARE REQUIRED

CPU board, RAM board, XU1707/1709 hard disk unit (27/65 MB, single port) and G0363 controller.

PRELIMINARY WARNING

Data is destroyed when certifying or formatting using this program. A dump operation must be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.4.1 TEST DESCRIPTION

1. ASSIGN ALTERNATIVE TRACK

   Permits an alternative user track to be assigned as follows:

   a) Searches for an alternative track.

   b) Formats the faulty track to reflect its new status.

   c) Certifies the faulty track in order to establish if the faulty track has at least half of its sectors error free.

   d) Formats the first free alternative track to reflect its new status.

   e) Performs a summary certification by writing/verifying 50 times on the alternative track (via the faulty track address) in order to find any errors on the track and to verify that the re-allocation is correctly effected.

      Writes the pattern %0000 on the data field of the alternative track (again via the faulty track address) as a further test to verify that the faulty track has been correcly re-allocated.

2. SECTOR VERIFY

   Verifies a sector of a track by using a series of read operations.

   After 5 consecutive positioning errors a home operation is made to track 0.

3. SECTOR CERTIFY

   Certifies a sector of a track by performing a series of write and read operations using a test pattern.

   After 5 consecutive positioning errors a home operation is made to track 0.

   If a recoverable ecc error is calculated by the program, the error burst length is compared with that of the controller. If they do not match a hardware error is indicated.

   If the ECC error is recoverable a test is made to see that the error burst length is not greater than the value contained in standard 24.

4. DISK IMAGE

   Displays, the following (as a result of reading identifiers):

   a) The faulty tracks which have been assigned with alternative tracks.

   b) The alternative tracks assigned.

   c) The faulty alternative tracks.

5. DISPLAY SECTOR(S)

   Displays the data field of sector(s) in HEX and ASCII characters. Each group of four HEX characters represents 2 bytes of the data field. The corresponding ASCII characters are shown adjacent the HEX characters (1 ASCII char for 2 HEX chars). A dot is displayed when there is no equivalent ASCII character.
   The sectors are displayed one at a time when ENTER is hit.

6. DISPLAY ERMAP ETF

   Details the errors found by the manufacturers of the disk.

7. DISPLAY HISTORY MAP

   Displays the data exchange details, number of errors found (sect, cyl & HD), critical sectors etc.

8. EXIT

   Terminates program.

17.4.2 SERVICE AND ERROR MESSAGES

Before changing disk check the controller using the controller diagnostic test program.

TEST 1

If the test has been correctly concluded the following is displayed:

```
>>> OPERATION CORRECTLY ENDED !!
>>> TRACK CYL: XXX HD: YY
>>> IS ASSIGNED TO TRACK
>>> CYL: ZZZ HD: KK
```

If the test reveals critical conditions one of the following messages is displayed:

```
>> THERE ARE NO MORE ALTERNATIVE TRACKS
>> IN ORDER TO ASSIGN FAULTY TRACKS!
```

```
>> CRITICAL DISK SURFACE !!
>> TRACK CYL: XXX  HD: YY
>> HAS NOT X SECTOR(S) ERROR FREE !!
```

```
>>> WARNING !!! <<<
>> TRACK CYL: XXX HD: YY
>> ASSIGNED TO TRACK CYL: KKK HD:ZZ
>> IS NOT RELIABLE !!!
>> REPEAT OPERATION, PLEASE !!!
```

TEST 2

The following messages are displayed for each sector selected by the operator:

```
>>>> SECTOR READ SUMMARY <<<<
>>> CYL: XXX HD: YY SECT: KK
>>> IDENT. FIELD: WW.....W(xyy%)
>>> CYCLE(S): XXXX ERROR(S) ZZZ
-------------------------------
>>> DATA FIELD: WW..... W(xyy%)
>>> CYCLE(S): XXXX ERROR(S) ZZZ
>>> MAX CONSECUTIVE ERRORS    X
```

```
WHERE:
WW...W = IN TOLERANCE,
         OUT OF TOLERANCE
         or UNKNOWN
     x = > (greater than) yy
         or < (less than) yy
    yy = threshold value for
         max. number of errors
         entered by operator
```

TEST 3

The following messages are displayed for each sector selected by the operator:

```
>>>> SECTOR CERTIFY SUMMARY <<<<
>>> CYL: XXX HD: YY SECT: KK
>>> IDENT. FIELD: WW.....W(xyy%)
>>> CYCLE(S): XXXX ERROR(S) ZZZ
---------------------------------
>>> DATA FIELD: WW..... W(xyy%)
>>> CYCLE(S): XXXX ERROR(S) ZZZ
>>> MAX CONSECUTIVE ERRORS    X
```

WHERE:
WW...W = IN TOLERANCE, OUT OF TOLERANCE or UNKNOWN
x = > (greater than) yy or < (less than) yy
yy = threshold value for max. number of errors entered by operator

The following messages are displayed if a burst error greater than N bits is found on a track:

```
>>>> SECTOR READ SUMMARY <<<<
>>> CYL: XXX HD: YY SECT: KK
>>> IS CRITICAL SECTOR ON DATA FIELD
>>> ERROR BURST IS > N BITS !!
>>> UNKNOWN IDENTIFIER FIELD CONDITION !!
>>> IDENT. >>> CYCLE(S): YY ERROR(S): XX
>>>   DATA >>> CYCLE(S): XXXX ERROR(S) ZZZ
```

N.B. A track containing a sector with this type of error is considered faulty.

TEST 4

The following messages are displayed when disk image is selected:

```
TRACK CYL: XXX    HD: X
JJJJJJJ.....JJ
CYL : XXX   HD: X

>>> FREE ALTERNATIVE TRACK:XX
```

WHERE:
JJ.J = IS ASSIGNED TO TRACK, or IS NOT CORRECTLY ASSIGNED TO TRACK or IS NOT CORRECTLY FORMATTED or IS A FAULTY ALTERNATIVE TRACK

TEST 5

The following messages are displayed in test 5:

```
*****************************
CYL:       XX HD:  X  SECT: X
*****************************

XXXX XXXX ....XXXX      ZZ..Z          XXXX = data in hex
XXXX XXXX ....XXXX      ZZ..Z          ZZ = ASCII code
  :    :       :        :  :
  :    :       :        :  :
XXXX XXXX ....XXXX      ZZ  Z
```

TEST 6

The following messages are displayed in test 6:

```
>>> DATE: X/XX/XX
>>> HOUR: XX
>>> IDENT. ERMAP
>>> TOTAL ERROR(S)
    CYL. HD LENGTH DISP.
1.  XXX  X    X    XXXX
2.  XXX  X    X    XXXX
3.  XXX  X    X    XXXX
      :   :    :     :
      :   :    :     :
      :   :    :     :
X.  XXX  X    X    XXXX
```

TEST 7

The following messages are displayed in test 7:

```
DATA EXCHANGE (IN SECTORS)
FROM CPU TO PU.........:XXXX          XXXX = critical sectors
FROM PU TO CPU.........:XXXX
FROM PU TO CONTROLLER..:XXXX          YYYY = Total number of
ERROR NUMBER...........:YYYY                 error found

*****************************         Displayed only if there are
N.  CYL: HD:  ST:  DEFECTS            errors,
*****************************         where:
nnnn cccc  hh   ss   ZZZZZZZ          nnnn = error number
nnnn cccc  hh   ss   ZZZZZZZ          cccc = cylinder
 :         :          :               hh   = head
 :         :          :               ss   = sector
nnnn cccc  hh   ss   ZZZZZZZ          ZZZZ = '+'; '-'; '!'
                                             or 'NOT FOUND'
```

	+ = critical sectors in tolerance - = critical sectors out of tolerance ! = sectors to be reassigned due to to error rate greater than acceptable value NOT FOUND = condition not not identified by by program
+ : TOL. - :OUT OF TOL ! : TO BE REAL.	Displayed on diagnostic line only if there are errors (REAL. = REALLOCATED)
HISTORY TRACK NOT WRITTEN	Displayed only if there is no history track

OTHER MESSAGES:

- PU ## ABSENT
- PU ## NOT READY
- TRACK 0 UNREADABLE TRY TO INSTALL STD24
  PROGRAM ABORTS
- STD 24 RECORDED ON TRACK 0 NOT CORRECT
  TRY TO INSTALL STD24
  PROGRAM ABORTS
- UNRECOVERED POSITIONING ERROR
- LANDING ZONE POSITIONING ERROR: this error results when the HEAD is not correctly positioned on the LANDING ZONE at the end of the program.

17.5 HDC503: XU1707/1709 CONTROLLER & DRIVER DIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To test the controller when connected to the XU1707/1709 hard disk unit (HDU). The program does not, however, distinguish faults caused by the controller or the HDU. Tests using a known working unit (controller/HDU) will have to be made if faults are to be localised.

REQUIRED HARDWARE

CPU board, RAM board, XU17007/1709 (WREN1/2) hard disk unit (27/65 MB, single port) and G0363 controller.

NOTES:

1. Cylinder 0 sector 15 must contain STANDARD 24. Also the WRITE/READ diagnostic track (indicated by the STANDARD 24) must be error free if the tests are to be completed.

2. The tests 1 to 16 are carried out sequentially. It is not possible to exclude or alter the sequence of any test.

3. The disk unit connected to the controller, which is not included in the test, may be left connected and ON LINE.

OPERATING PROCEDURE

Refer to section 1.3.2.

TEST 1 SLOT TEST-CHECK TYPE AND BOARD ADDRESS

Checks if the HDC5 controller is in its correct slot position as selected by the operator and also the type of controller by reading the controller name.

TEST 2 GENERATE INTERRUPT AND TEST VECTORS

Checks the interrupt request logic.

TEST 3 PROGRAM HDC & WRITE/READ FIFO

Checks the part of the INPUT/OUTPUT circuit associated with the FIFO memory.

TEST 4 TEST 8253 TIMER & DMA TRANSFER LOGIC

Checks the INPUT/OUTPUT circuit associated with the 8253 timer and the DMA transfer logic.

TEST 5 TEST DMA & RAM & ASS.ADDRESS COUNTER

The RAM addressing and storing functions are checked as well as the DMA address logic between the controller RAM and the system RAM.

TEST 6 - TEST HOME + TIMEROT + READID + STD24:CYL.0

Sector 15 of track 0 is accessed in order to identify the type of disk present, establish the operating parameters and make some initial tests.

TEST 7 TIME SEEK + TIMEROT + READID CYL. 0 TO END

Checks the driver positioning time from cylinder to cylinder, the rotation time and the ID's.

TEST 8 : READ/VERIFY READ CYL. ONLY; CYL.

Checks the contents of the read only diagnostic cylinder.

TEST 9 FORM-RD-VER. ERROR-FREE TRK CYL.

Tests the formatting and read logic on sectors of the ERROR FREE TRACKS using characters (e.g. gap, sync, ID, crc, data field, ecc etc.) generated by the controller board.

NOTE : IF THERE ARE NO ERROR-FREE TRACKS THE TEST IS SKIPPED.

TEST 10 READ IDENT. DIFF. TO STORED CYL.

Operates on the tracks of the read only diagnostic cylinder, sector 0.

Seaches for 'ERSE' errors caused by the search request for an ID different from the value recorded on the disk.

TEST 11 VERIFY DATA DIFF. TO READ CYL.

The first 9 sectors of each read only diagnostic cylinder, is tested by writing on these sectors and then verifying the data written.

TEST 12 WRITE-RD-VER.ERROR-FREE TRK CYL.

Tests the error-free tracks of the read/write diagnostic cylinder.

TEST 13 WR-RD-VER. NO-ERR.-FREE TRK CYL.

Tests as in previous test, except that the ERROR FREE tracks are ignored and only NON ERROR FREE tracks are used.

TEST 14 GENER. ERROR FOR ''ECC'' TEST CYL.

Operates on the ERROR FREE tracks of the write/read diagnostic cylinder. If there are NO ERROR FREE tracks the test is SKIPPED.

Checks the ECC generation-control logic differentiates between a recoverable and a non recoverable error, and that it successfully corrects a recoverable error.

The test is limited to sectors 0, 3 & 6.

TEST 15 FORM-WR-RD WITH WRONG IDENT.CYL.

Operates on the ERROR FREE tracks of the write/read diagnostic cylinder. If there are NO ERROR FREE tracks the test is SKIPPED.

checks that the ID control logic detects an ID formerly corrected in the search ID but stored on the driver with one or more different bit(s). This test differs from test 10 only in that the ID of test 10 is correct on the driver but different in the search ID.

The test is carried out on all the sectors of the error free tracks (maximum 2 tracks).

TEST 16 FORMAT-READ ''GPL2'' MINIMUM CYL.

Operates as described in test 9, but with different gap parameters.

These values are displayed when there is an error.

17.5.1 SERVICE AND ERROR MESSAGES

The following mesages can be displayed for errors not attributed to the controller board:

** PRIVILEGED INSTRUCTION TRAP **
** SEGMENT TRAP **
** NON MASKABLE INTERRUPT **

This message is displayed if an interrupt is not disabled with signal IRET active or if there are multiple interrupts:

** INTERRUPT NOT DISABLED **

TEST1 SLOT TEST-CHECK TYPE & BOARDS ADDRESS

THE SLOT ''X'' IS EITHER EMPTY OR
CONTAINS A NOT SELFDECLARING CONTROLLER

THE PRESENT CONTROLLER IN SLOT ''X''
ANSWER PHYSICAL NAME ''YY''
INSTEAD OF ''ZZ''

Replace the controller board if any OTHER error message is displayed.

TEST 2 to TEST 16

LIST OF ERROR MESSAGES TO BE SUPPLIED AT A LATER DATE

17.6 HDC5X3: ST506 HDU READ/WRITE ERMAP

PROGRAM PURPOSE

To format, read and write the tracks reserved for the ERMAP.

HARDWARE REQUIRED

CPU board, RAM board, ST506 hard disk unit (XU1707/ XU1709/ XU5006/ MICROPOLIS 1325 etc.) and G0363 controller.

PRELIMINARY WARNING

Data on ERMAP is destroyed when formatting using this program. A read operation or hard copy must be made if original data is to be preserved.

NOTES:

The ERMAP is located using data read from track 0, sector 15. Track 0 must therefore contain STANDARD 24 otherwise the program aborts.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.6.1 TEST DESCRIPTION

The program uses STANDARD 24 on track 0 sector 15 to define the ERMAP area and provides the following facilities:

FORMAT ERMAP TRACK

Formats the ERMAP track cancelling any previous data recorded on the track and certifies the track by writing a test pattern 200 times and verifying after each write operation that the data has been correctly written.

DISPLAY ERMAP

Permits the contents of the ERMAP to be displayed showing cylinder, head, length (in bits) and displacement (in bytes) associated with the defects.

WRITE ERMAP

Permits data to be written on the ERMAP overwriting existing data.

MODIFY ERMAP

Permits existing data on the ERMAP to be modified and additional data to be included.

EXIT

Permits the program to exit MENU and return to MONITOR

17.6.2 SERVICE AND ERROR MESSAGES

Before changing the disk the controller should be checked using the CONTROLLER diagnostic test program.

The following errors can be caused by the controller:

- >>> CONTROLLER INITIALISATION ERROR
- INCOHERENT CONTROLLER RESPONSE
- HARDWARE FAILURE
- >>> SECTOR IDENTIFIER NOT FOUND
- >>> DATA FIELD NOT FOUND
- >>> WRONG CYLINDER SELECTED
- >>> UNKNOWN CYLINDER SELECTED
- >>> WRONG HEAD SELECTED
- >>> CYL POSITION LOST DURING I/O OP.
- >>> ECC ERROR ON DATA FIELD
- >>> VERIFY ERROR ON FORMAT COMMAND

The following errors can be caused by the DISK UNIT (and should be replaced if not corrected):

- PU XX ABSENT
- PU XX NOT READY
- PU ERROR
- STD 24 RECORDED ON TRACK 0 NOT CORRECT
  TRY TO INSTALL STD 24

- PROGRAM ABORTS
- THE ERMAP IS EMPTY!!
- >>> ERMAP ABSENT!!!
- TRACK 0 UNREADABLE! TRY TO INSTALL STD24
  PROGRAM ABORTS
- ERMAP NOT READABLE
- ERMAP NOT WRITABLE
- ERMAP NOT FORMATTABLE
- ERMAP OVERFLOW
- ERROR IN CERTIFY TRACK
- LANDING ZONE POSITIONING FAILURE
- TIME OUT DURING I/O OPERATION
- HOME ERROR (check also the controller)
- SEEK ERROR (check also the controller)

17.7 S24W16: WRITE STANDARD 24 ON XU 1707 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

CPU board, RAM board, XU 1707(WREN1) hard disk unit (27MB, single port) and G0363 controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.7.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.7.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the S24X62 program.

17.8 S24W25: WRITE STANDARD 24 ON XU 1709 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

CPU board, RAM board, XU 1709 (WREN2) hard disk unit (65 MB, single port) and G0363 controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.8.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.8.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the SW24X62 program.

17.9 S24M54: WRITE STANDARD 24 ON MICROPOLIS 1325 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

CPU board, RAM board, MICROPOLIS 1325 hard disk unit (65 MB, single port) and G0363 controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.9.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.9.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the S24X62 program.

17.10 S24X11: WRITE STANDARD 24 ON XM5221 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

CPU board, RAM board, XM5221 hard disk unit (20 MB, single port) and G0363 controller.

OPERATING PROCEDURES Refer to section 1.3.2.

17.10.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.10.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the S24X62 program.

17.11 S24WD0: WRITE STANDARD 24 ON WREN2 41 MB HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

CPU board, RAM board, WREN2 hard disk unit (41 MB) and G0363 controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.11.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.11.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the S24X62 program.

17.12 S24MA1: WRITE STANDARD 24 ON MICROPOLIS 1323/A (40MB) HDU

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

MICROPOLIS 1323/A (40 MB) hard disk unit and G0363 controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.12.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.12.2 SERVICE AND ERROR MESSAGES Refer to section 14.8.2 of the S24X62 program.

17.13 S24MA1: WRITE STANDARD 24 ON NEC5126H HDU

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

HARDWARE REQUIRED

NEC5126H hard disk unit and G0363 controller.

OPERATING PROCEDURE

Refer to section 1.3.2.

17.13.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on\sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

17.12.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the S24X62 program.

18. HDU TEST PROGRAMS FOR ESDI INTERFACE

18.1 ESDIF3: G0404 AND G0405 DISK FORMATTER PROGRAM

PROGRAM PURPOSE

To format the hard disk unit (HDU) when connected to the ESDI Interface.

NOTE

This program is valid for the M30, M40 and M60 systems.

REQUIRED HARDWARE

G0404 and G0405 controller boards and one of the following HDUs: CDC WREN3 140MB, MICROPOLIS 1355 140MB or FUJITSU M2246 140MB.

PRELIMINARY WARNING

1) The program can only be run on a disk which contains data defined by STANDARD 24 on track 0.
2) Any data on the disk before formatting is lost.
3) The disk must be certified by the manufacture and have at least one ermap otherwise formatting is NOT carried out.

OTHER NOTES:

The program uses the ermap to allocate alternative tracks. Any errors found which is NOT in the ermap is indicated by an appropriate error message. Reference should then be made to the "verify and correction" program to allocate alternative tracks manually.

Formatting time : approx. 20 minutes for 140 MB.

OPERATING PROCEDURES

See section 1.3.2.

18.1.1 TEST DESCRIPTION

Refer to HDC5F5 program section 17.1.1

18.1.2 ERROR AND SERVICE MESSAGES

Refer to chap 17.1.2

18.2 ESDIE1: G0404 AND G0405 ERROR RATE PROGRAM

PROGRAM PURPOSE

To measure the error rate of the HDU under critical operating conditions when connected to an ESDI subsystem.

HARDWARE REQUIRED

G0404 and G0405 controller boards and one of the following HDUs: CDC WREN3 140MB, MICROPOLIS 1355 140MB or FUJITSU M2246 140MB.

NOTE This program is valid for M54, M64 and M70 systems.

PRELIMINARY WARNING

The write operation in this program destroys data present on the disk. A dump operation should be made before commmencing tests if data is to be preserved.

OPERATING PROCEDURES

Refer to section 1.3.2.

18.2.1 TEST DESCRIPTION

Refer to the HDC5E7 program section 17.2.1

18.2.2 ERROR AND SERVICE MESSAGES

Refer to section 17.2.2

18.3 ESDIV2: G0404 AND G0405 VERIFY AND CORRECTION PROGRAM

PROGRAM PURPOSE

To display the contents of the HDU data field and condition of disk (contents of factory ERMAP, list of alternative tracks used etc.), verify and certify tracks and sectors, and also assign and format alternative tracks.

This program is valid for the M30, M40 and M60 systems.

REQUIRED HARDWARE

G0404 and G0405 controller boards and one of the following HDUs: CDC WREN3 140MB, MICROPOLIS 1355 140MB or FUJITSU M2246 140MB.

PRELIMINARY WARNING

Data is destroyed when certifying or formatting using this program. A dump operation must be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

OPERATING PROCEDURES

See section 1.3.2.

18.3.1 TEST DESCRIPTION

1. ASSIGN ALTERNATIVE TRACK

   Permits an alternative user track to be assigned as follows:

   a) Searches for an alternative track.

   b) Formats the faulty track to reflect its new status.

   c) Certifies the faulty track in order to establish if the faulty track has at least half of its sectors error free.

   d) Formats the first free alternative track to reflect its new status.

   e) Performs a summary certification by writing/verifying 50 times on the alternative track (via the faulty track address) in order to find any errors on the track and to verify that the re-allocation is correctly effected.

      Writes the pattern %0000 on the data field of the alternative track (again via the faulty track address) as a further test to verify that the faulty track has been correcly re-allocated.

2. ASSIGN ALTERNATIVE SECTOR

Permits an alternative sector to be assigned as follows:

a) Searches for an alternative sector.

b) Formats the track with the selected sector treated as a faulty sector.

c) Certifies the track with 50 cycles of write/verify operations.

d) Writes the pattern %0000 on the data field of the track containing the faulty sector as a further test to verify that the faulty sector has been correcly re-allocated.

3. DISK IMAGE

Displays, the following (as a result of reading identifiers):

a) The faulty tracks which have been assigned with alternative tracks.

b) The alternative tracks assigned.

c) The faulty alternative tracks.

d) Any errors found during the program run time.

4. DISPLAY SECTOR(S)

Displays the data field sectors in HEX and ASCII characters. Each group of four HEX characters represents 2 bytes of the data field. The corresponding ASCII characters are shown adjacent the HEX characters (1 ASCII char for 2 HEX chars). A dot is displayed when there is no equivalent ASCII character.

5. DISPLAY HISTORY TRACK

Displays data exchange details, number of errors found (cyl, sect. & HD), critical sectors etc.

6. EXIT

Terminates program.

18.3.2 SERVICE AND ERROR MESSAGES

Unless otherwise stated check the controller then the disk unit if there are errors. Also note that not all service messages have been reproduced in this section as they have already been described in TEST PROCEDURES.

TEST 1

If the test has been correctly concluded the following is displayed:

```
>>> OPERATION CORRECTLY ENDED !!
>>> TRACK CYL: XXX HD: YY
>>> IS ASSIGNED TO TRACK
>>> CYL: ZZZ HD: KK
```

If the test reveals critical conditions one of the following messages is displayed:

```
>> THERE ARE NO MORE ALTERNATIVE TRACKS
>> IN ORDER TO ASSIGN FAULTY TRACKS!

>> CRITICAL DISK SURFACE !!
>> TRACK CYL: XXX  HD: YY
>> HAS NOT X SECTOR(S) ERROR FREE !!

>>> WARNING !!! <<<
>> TRACK CYL: XXX HD: YY
>> ASSIGNED TO TRACK CYL: KKK HD:ZZ
>> IS NOT RELIABLE !!!
>> REPEAT OPERATION, PLEASE !!!
```

TEST 2

The following messages are displayed if a sector is assigned correctly:

```
>>> OPERATION CORRECTLY ENDED!!
```

If an alternative sectors has NOT been found the following message is displayed:

```
>>>> WARNING !!! <<<
>>> TRACK CYL: XXX HD: YYY
>>> ALTERNATIVE SECTOR NOT AVAILABLE
>>> ASSIGN ALTERNATIVE TRACK, PLEASE !!!
```

If an error is found during certification phase the following is displayed:

```
>>>> WARNING !!! <<<
>>> TRACK CYL: XXX HD: YYY
>>> IS NOT RELIABLE !!!
```

TEST 3

The following messages are displayed when disk image is selected:

```
TRACK CYL: XXX    HD: X
JJJJJJJ.....JJ
CYL : XXX   HD: X

>>> FREE ALTERNATIVE TRACK:XX
```

WHERE:
JJJJ..JJ =
IS ASSIGNED TO TRACK,
or
IS NOT CORRECTLY
ASSIGNED TO TRACK
or
IS NOT CORRECTLY
FORMATTED
or
IS A FAULTY
ALTERNATIVE TRACK !!
or
ALTERNATIVE SECTOR
NOT AVAILABLE !!
or
ORIGINAL WRONG
SECTOR: XXX /
ALTERNATIVE

TEST 4

The following messages are displayed in test 5:

```
*****************************
CYL:XX HD:X  SECT:X  BYTE:ZZ
*****************************
XXXX XXXX ....XXXX      ZZ..Z
XXXX XXXX ....XXXX      ZZ..Z
  :    :        :        :  :
  :    :        :        :  :
XXXX XXXX ....XXXX      ZZ  Z
```

XXXX = data in hex
ZZ = ASCII code

TEST 5

The following messages are displayed in test 5:

```
** DISPLAY HISTORY TRACK  **
       CONTENTS
DATA EXCHANGE (IN SECTORS)
FROM CPU TO PU.........:XXXX
FROM PU TO CPU.........:XXXX
FROM PU TO CONTROLLER..:XXXX
ERROR NUMBER...........:YYYY
```

XXXX = critical
sectors

YYYY = Total number
of error found

The following is displayed if there are errors:

```
*****************************
  N.  CYL: HD:  ST:  DEFECTS
*****************************
nnnn cccc  hh   ss   ZZZZZZZ
nnnn cccc  hh   ss   ZZZZZZZ
 :          :          :
 :          :          :
nnnn cccc  hh   ss   ZZZZZZZ
```

where:
nnnn = error number
cccc = cylinder
hh = head
ss = sector
ZZZZ = '+'; '-'; '!'

\+ = critical sectors in tolerance
\- = critical sectors out of tolerance
! = sectors to be reassigned due to error rate greater than acceptable value

NOT FOUND =condition not identified by program

```
+ : TOL. - :OUT OF TOL
! : TO BE REAL.
```

Displayed on diagnostic line.

OTHER MESSAGES:

- PU ## ABSENT - verify disk/controller
- PU ## NOT READY - verify disk/controller
- TRACK 0 UNREADABLE TRY TO INSTALL STD24
  PROGRAM ABORTS
- STD 24 RECORDED ON TRACK 0 NOT CORRECT
  TRY TO INSTALL STD24
  PROGRAM ABORTS
- UNRECOVERED POSITIONING ERROR -verify disk/controller

18.4 ESDIT1: G0404 AND G0405 - DIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To test the controller when connected to a hard disk unit (HDU). The program does not, however, distinguish faults caused by the controller or the HDU. Tests using a known working unit (controller/HDU) will have to be made if faults are to be localised.

REQUIRED HARDWARE

G0404 and G0405 controller boards and one of the following hard disk units: CDC WREN3 140MB, MICROPOLIS 1355 140MB or FUJITSU M2246 140MB.

NOTES:

1. Cylinder 0 sector 15 must contain STANDARD 24. Also the WRITE/READ diagnostic track (indicated by the STANDARD 24) must be error free if the tests are to be completed.

2. The disk unit connected to the controller, which is not included in the test, may be left connected and ON LINE.

LOADING PROCEDURE

Refer to section 1.3.2.

18.4.1 TEST DESCRIPTION

TEST 1 SYSTEM TYPE TEST

Checks the type of controller conneted by reading the TIPO gate. If the gate responds correctly then the board selection logic, the BDA07 - BDA00 BUS, the OLIBUS timing logic and the OLIBUS communication buffer are checked.

TEST 2 GENERATE INTERRUPT AND TEST VECTORS

Checks the logic which generates and enables the interrupt request(s) by testing that all the even vectors output correctly. Initially the internal logic which generates the interrupts are tested and finally the generation of the individual vectored interrupts are checked.

TEST 3 FLAG TEST

Checks all the input flags by changing the input parameters one at a time and at each change verifying that the output parameters correspond.

At the end of the tests all the input flags are set to 0 (hence the corresponding outputs are set to 0) in order to reset the controller.

If there are any errors the input and output parameters are displayed in order for the operator to determine the incorrect flag.

TEST 4 TIMER TEST

Checks channel 0 and channel 1 of the 8253 timer and associated INPUT/OUTPUT circuit.

The 8253 component is programmed in timer mode with different values set on the input channels. For each value set the time taken for the interrupt request to be made is checked against acceptable values. Also a test is made to check that an interrupt is generated within a minimum time after time out.

TEST 5 BUFFER CHECK TEST

Checks the 24k byte local buffer using I/O routines as follows:

Loads various test patterns on whole of the 24 k buffer and then checks word for word the pattern used for the load operation with the pattern read using a store operation. This operation is repeated in loop mode after each load-store operation on a different data field. Between each loop test the data read during the store operation is erased to ensure that the data read is the result of the store operation.

TEST 6 - DMA POINTER TEST

Checks that the DMA functions correctly on every available system adddress.

The test comprises determining the available physical segments, preparing this area to receive data, effecting a store operation on this area, reading the data stored and verifying the data read with the data used for writting.

TEST 7 DMA LENGTH TEST

Checks that the controller can transfer blocks of 512 bytes, starting with 1 block then 2 blocks, etc. incrementing the number of blocks to be transfered to a maximum of 48 blocks so that a total of 24k bytes are transfered.

If the test is successful then channel 2 of the 8253 timer (which controls the DMA transfer length) is operating correctly.

TEST 8: DMA TRANFER SPEED TEST

Checks that the DMA can operate at 2 different speeds. A load operation is performed on a buffer of 24k bytes first with the DMA operating at a slow speed and then with the DMA operating at a fast speed. The time taken for each operation is checked and against standard values.

TEST 9: PU SELECTION TEST

Checks that the Peripheral Unit (i.e. disk) is accessable and operative. The PU selection circuit (HDSEL) is tested and the comfirmation (REUSA) signal is also checked.

TEST 10: PU COMMAND CABLE TEST

Verifies that the cicuit which communicates with the PU (command and PU status circuit) operates correctly.

TEST 11: SEEK CIRCUITRY TEST

Checks that the interrupt 'end of seek' functions correctly. A home routine is initiated, then the RESKx, ESKx and SKExN signals checked.

TEST 12 ATTENTION TEST

Generates an error and verifies if the system recovers the error.

TEST 13 PU DIAGNOSTIC TEST

Performs a diagnostic test on the PU and checks to see if there are any errors.

TEST 14 STANDARD 24 VERIFICATION TEST

Initialises the PU, reads the STANDARD 24 and hence establishes if the PU can be connected. The function of the test is also to verify the read logic. This test must be made before any of the following tests can be carried out.

TEST 15 SEEK TEST

Verifies that the drive is correctly positioned on the read only cylinder and that the information contained in the ID's of sector 0 is coherent.

TEST 16 MULTISECTOR VERIFICATION TEST

Reads the Read Only Diagnostic Cylinder and verifies if the system can perform the multisector commands.

TEST 17 HEAD SELECTION TEST

Verifies that the head selection logic functions correctly.

TEST 18 VERIFY CIRCUITRY TEST

Launches a verify command and checks that the system replies with an ERCE error signal (typical error of a memory buffer different from that on the disk). If this signal is not generated then an error message is displayed.

TEST 19 DIAGNOSTIC BAD SECTORS LOCATION

Reads sector 15 of the Read Only cylinder in order to obtain the information neccessary (location of bad sectors) to operate on the Diagnostic Write cylinder.

TEST 20 FORMAT AND READ PHYSICAL TEST

Formats the Write Diagnostic cylinder, followed by a physical read on each sector verifying that the sector has been correctly formatted and that the ID's correspond.

TEST 21 WRITE TEST

Writes and verifies the patterns 00, FF and A5 on all the sectors of the Write Test cylinder.

TEST 22 WRITE PHYSICAL TEST

Writes the pattern 00, FF and A5 on the first error free physical sector of the write diagnostic cylinder using a write physical operation. This is then followed by a load operation of the controller buffer and finally followed by a physical read of the same sector to see if the data written is the same as the data read.

TEST 23 TEST PHYSICAL TEST

Tests that the physical sector functions correctly in the same way as the previous test using the same test patterns but in this case the test is effected using the physical sector test instead of the physical read, store and comparison test.

It is necessary to know the location of the faulty sectors which have been re-allocated as this would give misleading results.

TEST 24 BEP (BURST ERROR PROCESSOR) TEST

Checks if the Burst Error Processor can test correctly the ECC data field and if errors are found, determines the correct location of the error and corrects the error if possible. The test is effected only on the first good sector found of head 2 of the diagnostic write cylinder.

It is necessary to know the location of the faulty sectors which have been re-allocated as this would give misleading results.

TEST 25 ID ERROR MANAGMENT TEST

Tests that the logic which determines errors using the ID's (ERSE, ERPO, ERSY and ERWO) functions correctly.

It is necessary to know the location of the faulty sectors which have been re-allocated as this would give misleading results.

A write physical operation is performed on the diagnostic write cylinder, introducing errors which are then comfirmed with successive physical reads.

18.5 EIW353: WRITE STANDARD 24 ON CDC WREN3 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

REQUIRED HARDWARE

G0404 and G0405 controller boards and WREN3 HDU (140MB).

OPERATING PROCEDURES

See section 1.3.2.

18.5.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

18.5.2 ERROR AND SERVICE MESSAGES

Refer to chap 14.8.2

18.6 EIM5S3: WRITE STANDARD 24 ON MICROPOLIS 1355 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

REQUIRED HARDWARE

G0404 and G0405 controller boards and MICROPOLIS 1355 140MB HDU.

OPERATING PROCEDURES

See section 1.3.2.

18.6.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

18.6.2 SERVICE AND ERROR MESSAGES

Refer to section 14.8.2 of the S24X62 program.

18.7 EIF653: WRITE STANDARD 24 ON FUJITSU M2246E HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

REQUIRED HARDWARE

G0404 and G0405 controller boards and FUJITSU M2246E 140MB HDU.

OPERATING PROCEDURES

See section 1.3.2.

18.7.1 TEST DESCRIPTION

The program comprises two routines depending on the operator's selection:

1. Certification and formatting of track 0 and recording of data defined by STANDARD 24 on the same track:

   a) Track 0 is read to check that it is NOT formatted and does NOT contain a recording of STANDARD 24.

   b) Track 0 is certified in order to detect the number of bad sectors; if this number is more than 5 the program aborts.

   c) STANDARD 24 data is recorded on track 0.

2. Recording of the relative part of STANDARD 24 on sector 15:

   1. Track 0 is read to check that it is already formatted and contains a recording of STANDARD 24.

   2. The SECTOR IDENTIFIER field is checked to see that it contains the expected data.

   3. The UNIT NAME and RELEASE fields are checked to see that they contain the expected data.

   4. The relative part of STANDARD 24 is recorded on sector 15.

In both cases a summary message is displayed to indicate any errors or if the program has been correctly executed.

18.7.2 SERVICE AND ERROR MESSAGES Refer to section 14.8.2 of the S24X62 program.

18.8 EIM350: WRITE STANDARD 24 ON MICROPOLIS 1353 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

REQUIRED HARDWARE

G0404 and G0405 controller and MICROPOLIS 1353 70MB HDU.

OPERATIVE PROCEDURES

See section 1.3.2.

18.8.1 TEST DESCRIPTION

Refer to the S24X62 program section 14.8.2.

N.B. The contents of sector 15 is given in the following tables.

18.8.2 ERROR MESSAGES

Refer to section 14.8.3.

18.9 EIP650: WRITE STANDARD 24 ON PRIAM 638S HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

REQUIRED HARDWARE

G0404 and G0405 controller and PRIAM 638 315MB HDU.

OPERATIVE PROCEDURES

See section 1.3.2.

18.9.1 TEST DESCRIPTION

Refer to the S24X62 program section 14.8.2.

N.B. The contents of sector 15 is given in the following tables.

18.9.2 ERROR MESSAGES

Refer to section 14.8.3.

18.10 EIMBSO: WRITE STANDARD 24 ON MICROPOLIS 1558 HARD DISK UNIT

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 through to 15 of track 0, cylinder 0.

REQUIRED HARDWARE

G0404 and G0405 controller and MICROPOLIS 1558 315 MB HDU.

OPERATIVE PROCEDURES

See section 1.3.2.

18.10.1 TEST DESCRIPTION

Refer to the S24X62 program section 14.8.2.

N.B. The contents of sector 15 is given in the following tables.

18.10.2 ERROR MESSAGES

Refer to section 14.8.3.

19. HARD DISK UNIT (PATRIOT 9720 CDC VIA SMD3) TEST PROGRAMS

19.1 S3PTF2: PATRIOT 9720 CDC VIA SMD3 DISK FORMATTER PROGRAM

PROGRAM PURPOSE

To format the PATRIOT hard disk unit when connected to a SMD3 interface.

REQUIRED HARDWARE

G0301/A and G0302/A interface boards, PATRIOT 9720 EMD CDC hard disk unit (275 MB).

PRELIMINARY WARNING

The disk must be certified by the manufacturer and have at least one ermap otherwise formatting is carried out without assigning alternative tracks or initialising the data field.

Also note that any data on the disk before formatting is lost.

Formatting time : approx. 1 Hour.

LOADING PROCEDURES

Refer to section 1.3.2.

19.1.1 TEST DESCRIPTION

Refer to section 15.1.1 of the SM23F6 program.

19.1.2 ERROR MESSAGES

Refer to section 15.1.2.

EXAMPLE OF ERMAP

```
-------------FACTORY ERMAP ----------          x = 1, 2, 3 or 4
              USER AREA                         where:
TRACK  ERRATE CYL: XXX HD Y       TDIFx         1 = faulty sector
SECTOR ERRATE CYL: XXX HD Y SEC:Z TDIFx         2 = faulty track,
              SPECIAL AREA                      3 = faulty sector
TRACK  ERRATE CYL: XXX HD Y       TDIFx         on special track,
------------ FIELD ERMAP ------------           4 = track with no
              USER AREA                         PATRIOT status
TRACK  ERRATE CYL: XXX HD Y       TDIF2
SECTOR ERRATE CYL: XXX HD Y SEC:Z TDIF1
             SPECIAL AREA
```

19.2 S3PTS0: WRITE STANDARD 24 ON PATRIOT 9720 CDC VIA SMD3

PROGRAM PURPOSE

To write data defined by STANDARD 24 on sectors 7 and 12 of track 0, cylinder 0.

REQUIRED HARDWARE

G0301/A and G0302/A interface boards, PATRIOT 9720 EMD CDC hard disk unit (275 MB).

LOADING PROCEDURES Refer to section 1.3.2.

19.2.1 TEST DESCRIPTION

Refer to section 15.1.1 of the SM23F6 program.

19.2.2 ERROR MESSAGES

The error messages are the same as those listed in section 15.1.2 with the following exceptions:

- **TYPE C MESSAGES:**

  Only the SEEK INCOMPLETE or messages which refer to the DRIVE apply (i.e. DRIVE IN PERMANENT FAILURE etc.).

- **TYPE D MESSAGES:**

  Only the NO RESET INTERRUPT IN THE CONTROLLER applies.

19.3 S3PTE0: PATRIOT 9720 VIA SMD3 ERROR RATE PROGRAM

PROGRAM PURPOSE

To check the reading and writing operation of a PATRIOT hard disk unit when connected to a SMD3 subsystem and operating under normal user mode.

HARDWARE REQUIRED

G0301/A and G0302/A controller boards and PATRIOT 9720 EMD CDC hard disk unit (275 Mbytes).

PRELIMINARY WARNING

The write operation in this program destroys data present on the disk. A dump operation should be made before commmencing tests if data is to be preserved.

LOADING PROCEDURES

Refer to section 1.3.2

19.3.1 TEST DESCRIPTION

Refer to section 15.3.1 of the 2312E8 ERROR RATE program.

19.3.2 ERROR MESSAGES

The error messages are the same as those listed in section 15.3.2. with the following differences:

- **TYPE A MESSAGES**

  These messages apply also for WRITE operations.

- **TYPE C MESSAGES**

  Only messages which refer to the DRIVE apply.

- **TYPE C AND D MESSAGES**

  The following additional messages apply:

  . MAIN MEMORY DATA COMPARE ERROR
    HARDWARE FAILURE:
    ALL/SOME/WRONG DATA TRANSFRERED or WRONG BLOCK LABEL FOUND

  The "PARAMETER ERROR" and "INCOHERENT RESPOSE" messages do not apply.

19.4 S3PSD0: PATRIOT 9720 CDC HDU/SMD3 and STC SAVE-RESTORE PROGRAM

PROGRAM PURPOSE

To evaluate the error rate of the PATRIOT/SMD3 subsystems and the STC subsystem by writing and reading sample patterns under cririca l conditions and performing SAVE (disk to tape) and RESTORE (tape to disk) operations.

HARDWARE REQUIRED

PATRIOT 9720 EMD CDC hard disk unit (275 MB), G0301/A and G0302/A controller boards and streaming tape cartridge unit (STC), STC adaptor and controller.

PRELIMINARY WARNING

The write, save and restore operations in this program destroys data present on both disk and tape units. A dump operation on each unit should be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES Refer to section 1.3.2.

19.4.1 TEST DESCRIPTION

Refer to section 15.4.1 of the 235CT3 program.

19.4.2 ERROR MESSAGES

Refer to section 15.4.2

19.5 S3PTC0: PATRIOT 9720/SMD3 DRIVER - DIAGNOSTIC TEST PROGRAM

PROGRAM PURPOSE

To test the SMD3 controller boards when connected to 1, 2, 3 or 4 PATRIOT 9720 EMD CDC hard disk units.

REQUIRED HARDWARE

G0301/A and G0301/A controller boards, PATRIOT 9720 hard disk units (275 MB)

WARNING

The disk units connected to the SMD3 adaptor, which are not included in the test, may be left connected and ON LINE but must not be selected for the READ/WRITE test.

Cylinder 821 is reserved for the diagnostic tests. The cylinder must be formatted and must contain an OLIVETTI test program.

Cylinder 820 track 06 must not contain any errors.

NOTE

The tests 1 to 26 must be carried out sequentially with the exception of tests 15 to 16 which may be omitted if the following conditions are prevalent:

-test 15 ; the ram size is not known and the test gives an error,

-test 16 ; the reserved test cylinder is faulty.

LOADING PROCEDURES

Refer to section 1.3.2.

19.5.1 TEST DESCRIPTION

Refer to the SM0609 program section 15.5.1.

19.5.2 ERROR MESSAGES

Refer to section 15.5.2.

19.6 S3PTTO: PATRIOT 9720 CDC/SMD3 ROTATION TIME MEASUREMENT TEST

PROGRAM PURPOSE

To calculate the rotation and positioning time of the HDU.

HARDWARE REQUIRED

G0301/A and G0302/A controller boards, PATRIOT 9720 CDC (275MB) HDU.

LOADING PROCEDURES

Refer to section 1.3.2.

19.6.1 TEST DESCRIPTION

Refer to the F60TM3 program section 15.6.1.

N.B. In test 2, the positioning time taken is for 822 tracks (40ms).

19.6.2 ERROR AND SERVICE MESSAGES

N.B. Ensure disk is correctly formatted and has standard 24 installed.

If any of the following messages are displayed use the diagnostic program to verify the controller boards (if controllers OK replace HDU):

- HARDWARE/PERMANENT/TEMPORARY FAULT
- U.P. BUSY or NOT AVAILABLE/RECOGNISED
- TIME OUT ERROR MEMORY ACCESS
- MEMORY ERROR
- SYSTEM BUS ERROR
- INCOHERENT ANSWER
- TOO SMALL TO BE MEASURED

Use the verify and correction program to investigate fault if any of the following messages are displayed:

- ERROR ON "IDENTIFIER"/"READ COMMAND"
- "SECTOR"/"DATA MARK" NOT FOUND
- ERROR ON VERIFY

19.7 S3PTV0: PATRIOT 9720 CDC/SDM3 VERIFY AND CORRECTION PROGRAM

PROGRAM PURPOSE

To display the contents of the HDU data field and condition of disk (no. of faulty tracks, alternative tracks etc.), verify and certify tracks and sectors, and also assign and format alternative tracks.

HARDWARE REQUIRED

G0301/A and G0302/A controller boards, PATRIOT 9720 EMD CDC (275 MB) HDU.

PRELIMINARY WARNING

Data is destroyed when certifying or formatting using this program. A dump operation must be made if data is to be preserved or tests should be restricted to cylinders or tracks not containing valuable data.

LOADING PROCEDURES

Refer to section 1.3.2.

19.7.1 TEST DESCRIPTION

Refer to the SM12V4 program section 15.7.1.

19.7.2 SERVICE AND ERROR MESSAGES

TRACK STATUS MESSAGES

- FREE/BAD/ASSIGNED ALTERNATIVE TRACK
- GOOD/BAD USER TRACK
- TRACK WITH ALTERNATIVE SECTOR FREE
- ALTERN. SECTOR USED INSTEAD OF SECTOR: X
- ALTERNATIVE TRACK ASSIGNED TO
  FAULTY TRACK CYL: XX, HD: X
- FAULTY TRACK ASSIGNED TO
  ALTERNATIVE TRACK CYL: XX, HD: X

ERROR MESSAGES

N.B. Ensure disk is correctly formatted and has standard 24 installed.

If any of the following messages are displayed use the diagnostic program to verify the controller boards (if controllers OK replace HDU):

- PU BUSY/NOT READY/"IN WRITE PROTECTION CONDITION"

- ABSENT/UNKNOWN PU
- POSITIONING/TIME-OUT ERROR !!
- HARDWARE/SOFTWARE ERROR
- INCOHERENT REPLY
- MEMORY/SYSTEM BUS MEMORY ERROR
- PERIPHERAL CONTROL SYSTEM BUSY
- ERROR DURING READ/WRITE PHASE
- TEMPORARY/PERMANENT DRIVE FAILURE
- CONTROLLER AND ADAPTER BUSY
- CONTROLLER ABSENT/NOT RESET
- TOO MANY PU SELECTED !!
- WRONG ALTERNATIVE TRACK
- UNKNOWN CONTROLLER
- SEEK INCOMPLETE !!

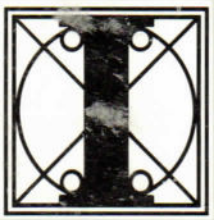
Replace HDU if any of the following messages are displayed:

- ECC/IDENTIFIER ERROR:
  ON CYL: xxx HD: xx SECT: xx
- SECTOR NOT FOUND:
  ON CYL: xxx HD: xx SECT: xx
- POSITIONING ERROR !!
  BEFORE INITIALIZATION PHASE
- DATA COMPARE OR VERIFY ERROR
  ON CYL: xxx HD: xx SECT: xx
- IDENTIFIER/DATA FIELD ECC ERROR
  ON CYL: xxx HD: xx SECT: xx
- MISSING DATA ADDRESS MARK
  ON CYL: xxx HD: xx SECT: xx
- WRONG TRACK WITHOUT ALTERNATIVE ASSIGN
  ON CYL: xxx HD: xx

DATE	UPDATED PAGES	PAGES	CODE
30-01-87	1st EDITION	488	4102230 T (0)
15-07-87	Pages to be replaced: Preface A, B, v-xxi, 1-7, 1-41, 1-42, 2-1, 2-5, 2-8, 2-11, 2-14, 2-17, 2-18, 3-7-3-10, 3-12, 3-13, 3-19 - 3-24, 3-25, 4-1 - 4-6, 4-16, 4-17, 5-1, 5-15 - 5-18, 7-6 - 7-12, 7-14, 7-16 - 7-20, 7-23, 8-28 - 8-36, 9-6, 9-9 - 9-33, 10-1, 10-13, 11-15, 11-22, 11-26, 12-1, 14-13, 15-13, 16-5, 17-6 Pages to be added: xxii, 3-24/1, 3-24/2, 3-27 -3-30, 4-6/1, 4-6/2, 4-16/1, 4-16/2, 5-19 - 5-23, 8-37 - 8-44, 17-37, Chap. 19 (All) Pages to be suppressed: 9-34 - 9-39*	179	4102231 U
29-02-88	Pages to be replaced: 2-1, 2-5, 2-8, 2-11, 2-14, 2-17, 3-8 - 3-14, 3-19, 3-21 - 3-30, 4-1, 4-7 - 4-45, 5-15, 7-6, 7-12, 7-16, 7-18 - 7-20, 8-41, 9-33, 11-26, 11-28, 18-1, 18-3 Pages to be added: 18-15 - 18-18 Pages to be suppressed: 9-34 - 9-39	123	4102232 G
30-03-88	Pages to be replaced: v - xxi, 3-8, 3-28, 4-1, 7-6, 7-9, 7-12, 7-14, 7-26 - 7-33 Pages to be added: 4-46 - 4-57	59	4102233 C
15-09-89	Pages to be suppressed: Preface B, vii, xii, xxii, xxiii, 3-8, 3-18, 3-29, 9-6, 18-16, 18-17 Pages to be added: 18-16, 18-17 Pages to be suppressed: 18-18*	21	4102234Z-00

Pages marked * must be suppressed

Code 4102230 T (0)
Printed in Italy



olivetti